

LCFC Confidential

BYG43

Lenovo Yoga 700 (14)

NM-A601 REV1.0

Haydn SKL M/B Schematics Document


INTEL SKYLAKE-U Platform

INTEL SKL U-series CPU + DDR3L DIMM+ NV N16S-GT

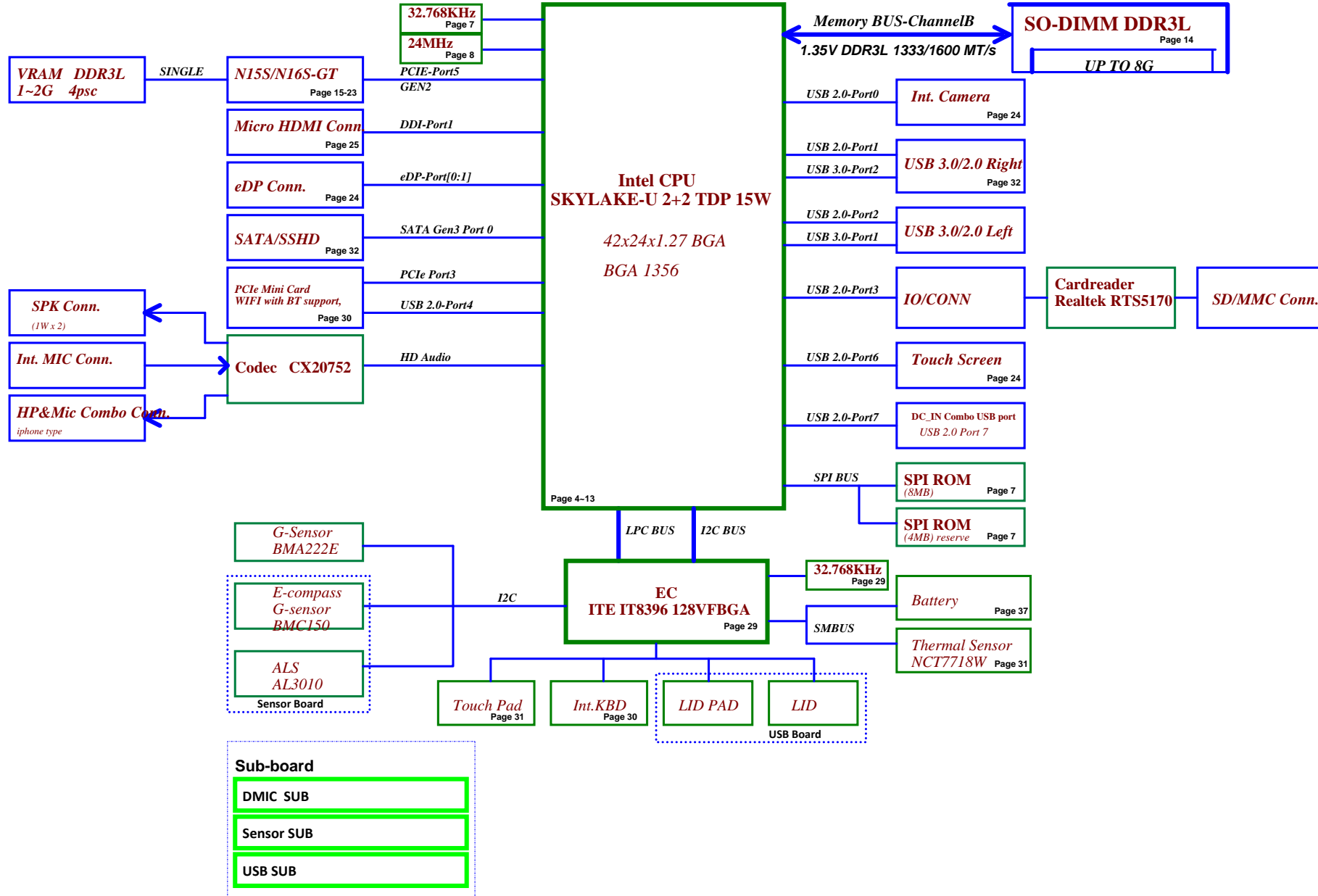
2015-07-20

REV:1.0

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Yoga 700(14) Block diagram



Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane State	B+ +3VL +5VLP	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.05VS +0.68VS +CPU_CORE	+1.35V_CPU
S0	O	O	O	O	O	O
S3	O	O	O	O	X	O
DS3	O	O	X	O	X	X
S5 S4/AC Only	O	O	O	X	X	X
S5 S4 Battery only	O	X	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
DS3 (Suspend to RAM)	LOW	LOW	HIGH	ON	LOW	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	Sensor	ALS	BATT	touch sensor	SODIMM	GPU	Thermal Sensor	PCH	charger
EC_SMB_CLK1 EC_SMB_DAT1	IT8386 +3VALW_BC	X	X	V +3VLP	X	X	X	X	X	V
EC_SMB_CLK3 EC_SMB_DAT3	IT8386 +3VS	V +3VS	V +3VS	X	X	X	X	X	X	X
EC_SMB_CLK0 EC_SMB_DAT0	IT8386 +3VS	X	X	X	X	X	V	V +3VS	V +3VALW_PCH	X
SMB_CLK SMB_DATA	PCH +3VALW_PCH	X	X	X	X	V +3VS	X	X	X	X

SM Bus address

	Device	address
EC1	Battery	0001_011X b
	Charger	
EC3	Sensor	
	ALS	
EC0	Thermal Sensor	1001_100xb
PCH	PCH THM	
	TP	

PCIE PORT LIST

Port	Device
1	X
2	X
3	WLAN
4	X
5	GPU

USB Port Table

	USB20	USB30
0	CAMERA	Left USB
1	Right USB	Right USB
2	Left USB	X
3	CARD READER	X
4	BT	
5	Sensor	
6	TOUCH PANEL	
7	DC_IN combo USB2.0	

BOM Structure Table

BOM Structure		BOM Structure	
DA8@	PCB	MIRROR@	EC Mirror-code enable
UMA@	UMA SKU part	UNMIRROR@	EC Mirror-code disableable
DEBUG@	DEBUG CARD Part	OPT@	Discrete GPU SKU part
ME@	ME part(connector, hole)	N15SGT@	For N15S-GT GPU part
RF@	RF request	GC6@	GC62.0 support part
EMC@	EMC request	RANKA@	For VRAM RankA part
CD@	COST DOWN Part		
REV@	RESERVER Part		

BOM Configuration Table

SKU	Description	BOM Config
SKU1		
SKU2		

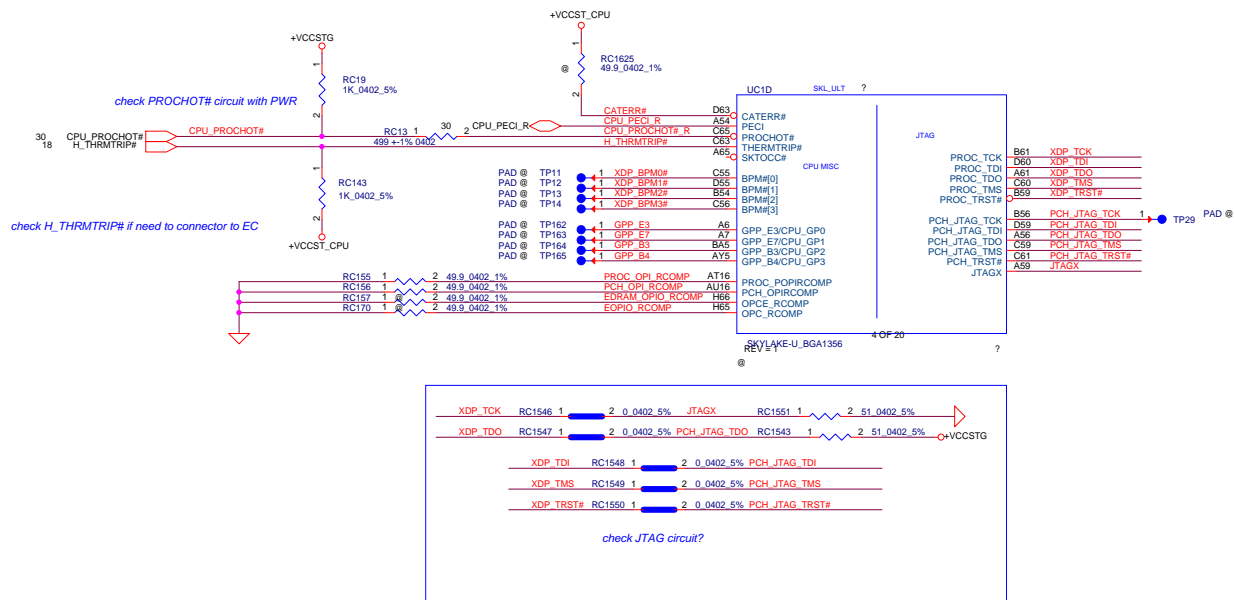
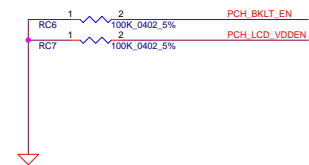
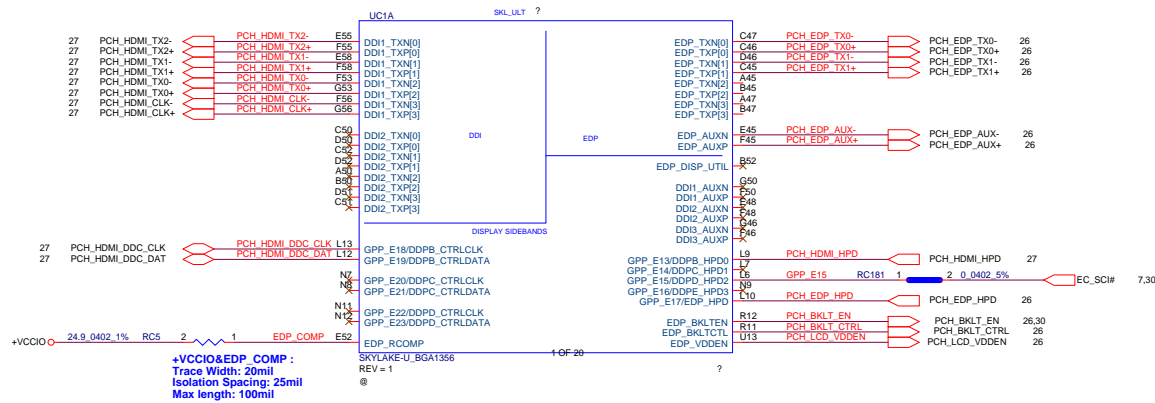
X76&VGA Configuration Table

SKU	Description	BOM Config

PCB And LOGO Config

PCB	ZZZ3 DA8@ PCB BYG43 NM-A601 NS-A601/A602	LOGO
CPU	ZZZ1 2.3G@ Intel i5-6200U 2.3G/2C/3M ZZZ2 2.5G@ Intel i7-6500U 2.5G/2C/4M	ZZZ4 HDMI@ HDMI LOGO ZZZ5 USB30@ USB30 LOGO
VRAM	ZZZ6 HY2G@ HYNIX 2G ZZZ7 MIC2G@ MICRON 2G ZZZ8 SAM2G@ SAMSUNG 2G	

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DDP*_CTRLDATA strapping sampled on the rising edge of PWROK

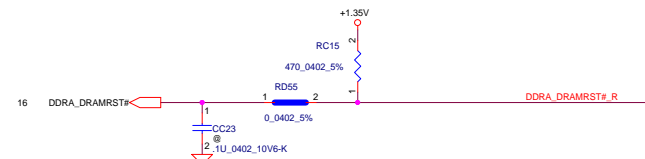
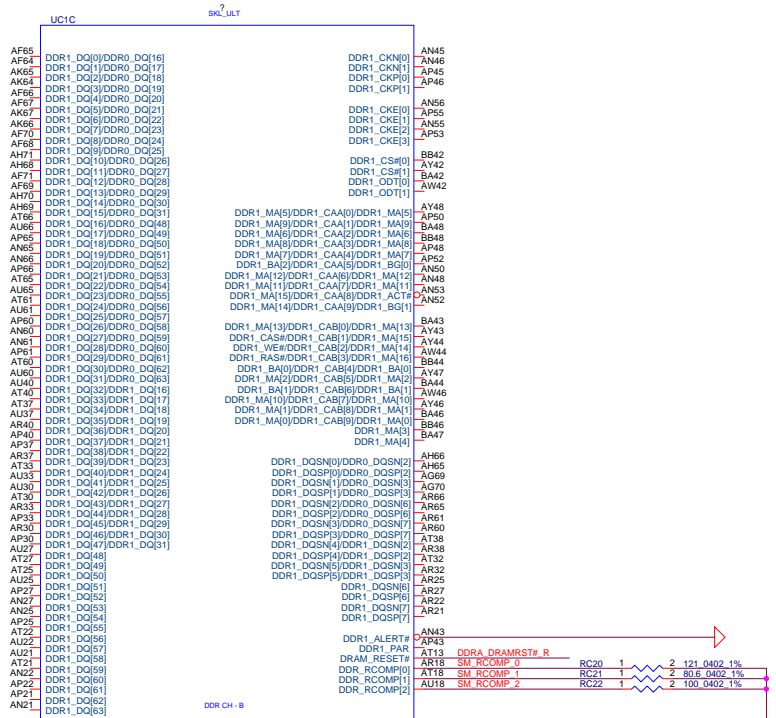
Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2kOhm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2kOhm	NC


Port	DDI PROCESSOR	Pin Names	HDMI* Mapping
Port 1	DDI1_TXN[0]	DDI1_TXN[0]	HDMIx_TX2_DN
	DDI1_TXP[0]	DDI1_TXP[0]	HDMIx_TX2_DP
	DDI1_TXN[1]	DDI1_TXN[1]	HDMIx_TX1_DN
	DDI1_TXP[1]	DDI1_TXP[1]	HDMIx_TX1_DP
	DDI1_TXN[2]	DDI1_TXN[2]	HDMIx_TX0_DN
	DDI1_TXP[2]	DDI1_TXP[2]	HDMIx_TX0_DP
	DDI1_TXN[3]	DDI1_TXN[3]	HDMIx_CLK_DN
	DDI1_TXP[3]	DDI1_TXP[3]	HDMIx_CLK_DP
	DDPB_HPD	DDI1_HPD_Q	
	DDPB_CTRLCLK	DDI1_CTRL_CLK	
	DDPB_CTRLDATA	DDI1_CTRL_DATA	

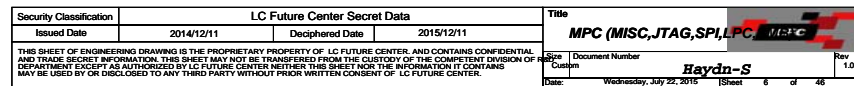
DisplayPort* Disabling and Termination

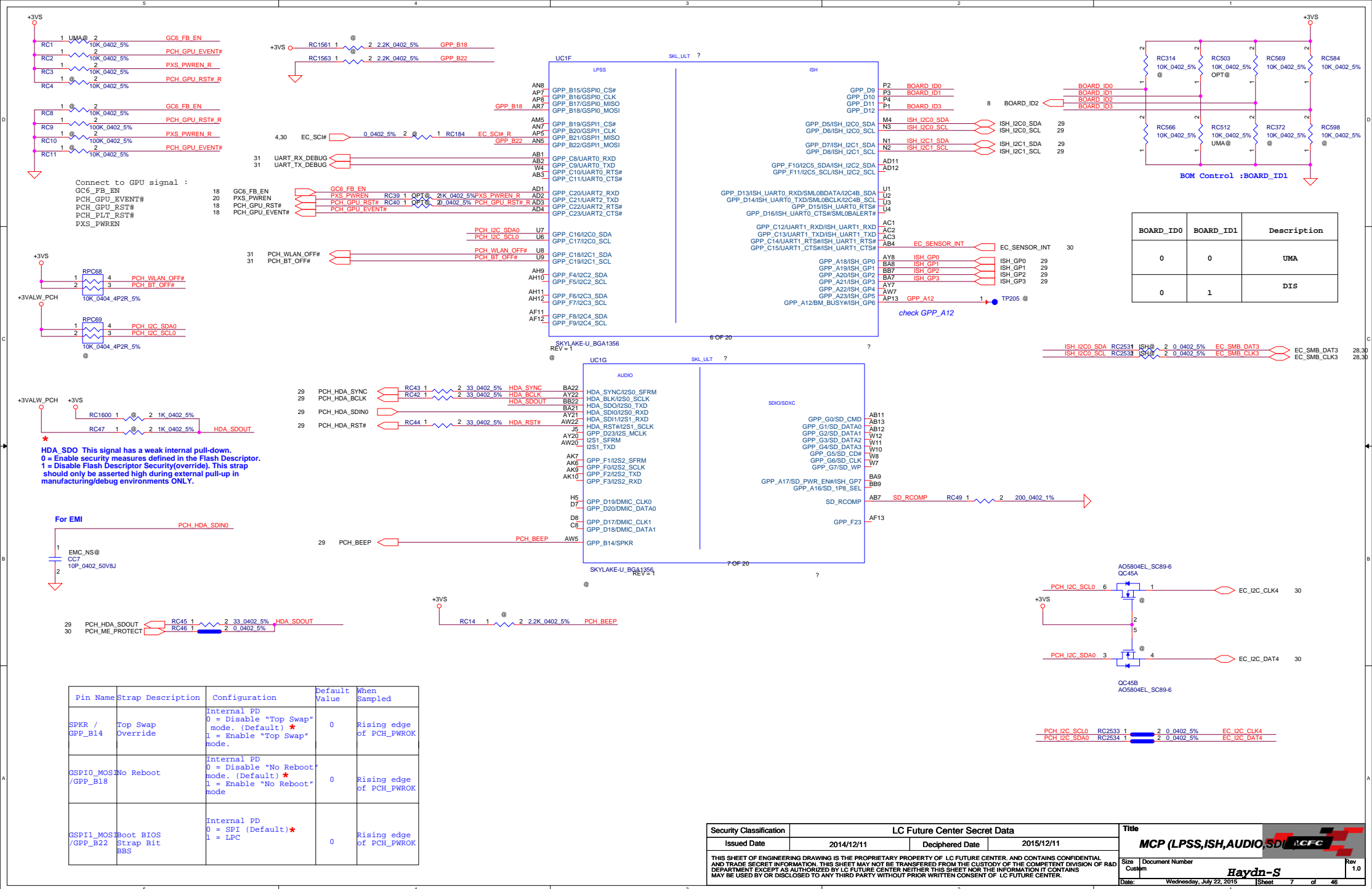
Pin Name	Recommendation
DDPC_AUXP	No Connect
DDPC_AUXN	No Connect
DDPC_HPD	No Connect
DDI2_TXP[3:0]	No Connect
DDI2_TXN[3:0]	No Connect
DDPC_CTRLCLK	No Connect
DDPC_CTRLDATA	No Connect

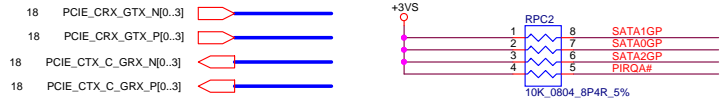
	DDRA_DQ[63:0]	16
	DDRA_DQS[7:0]	16
	DDRA_DQS#[7:0]	16



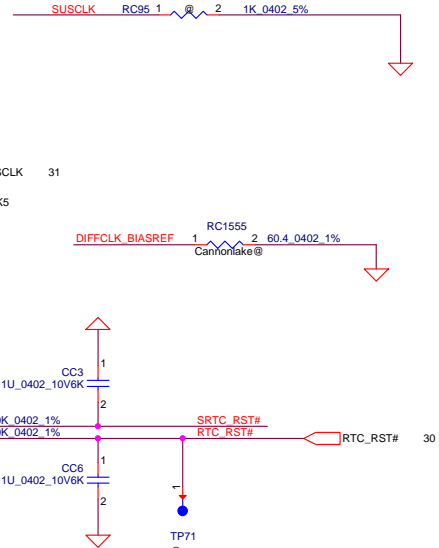
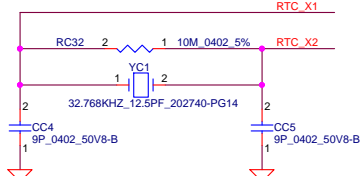
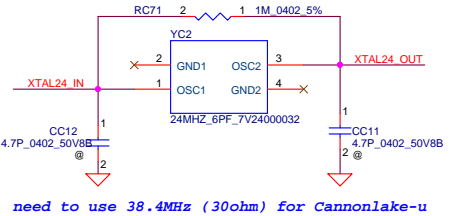
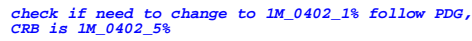
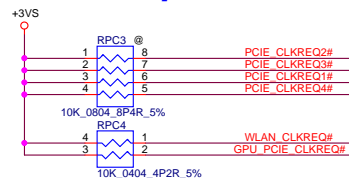
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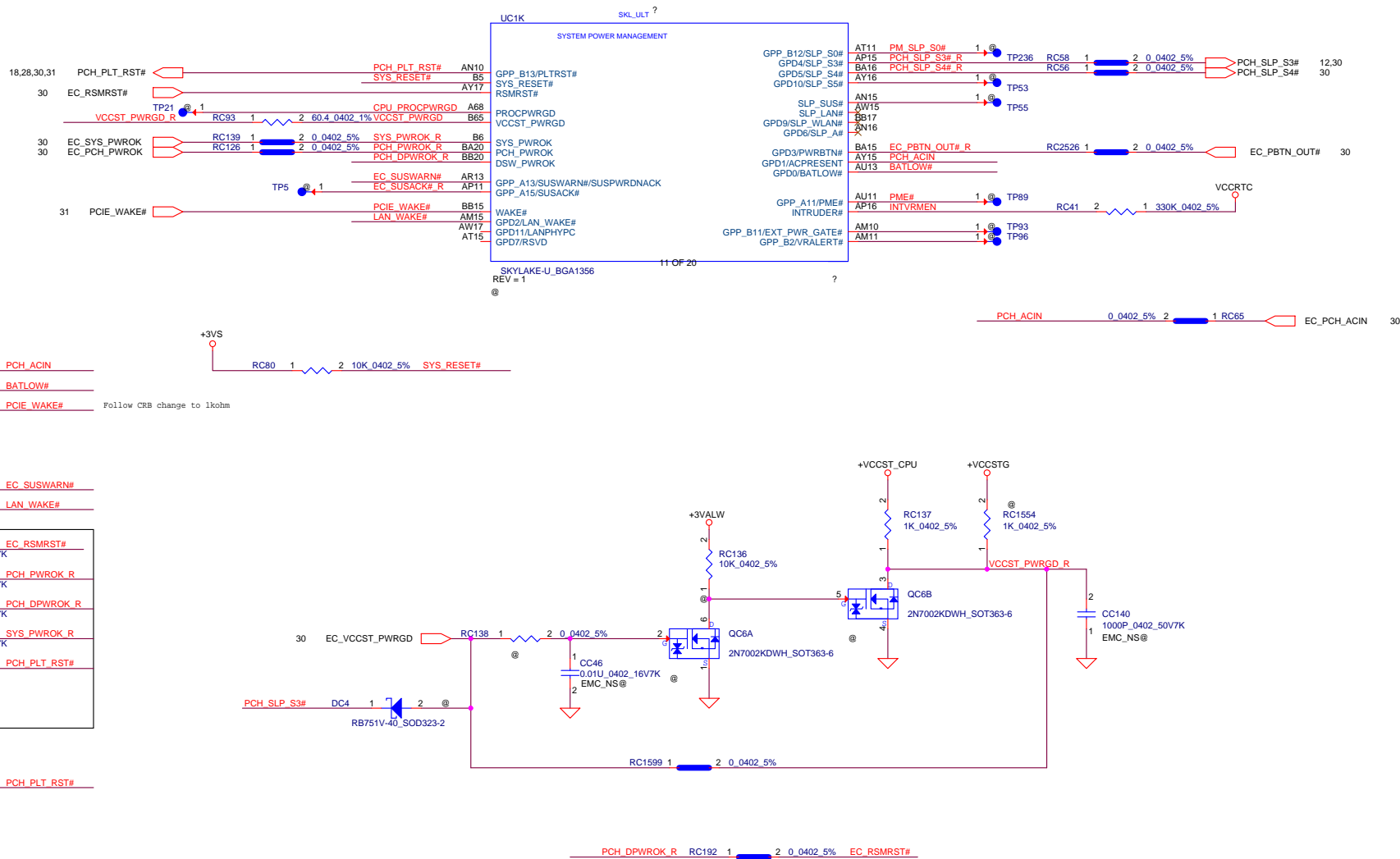


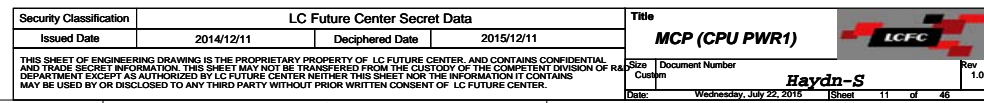
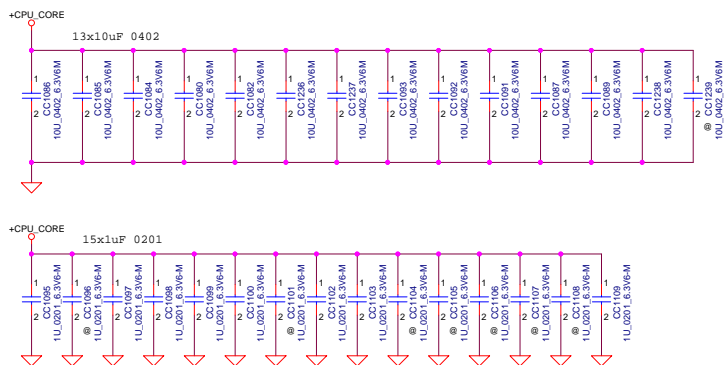


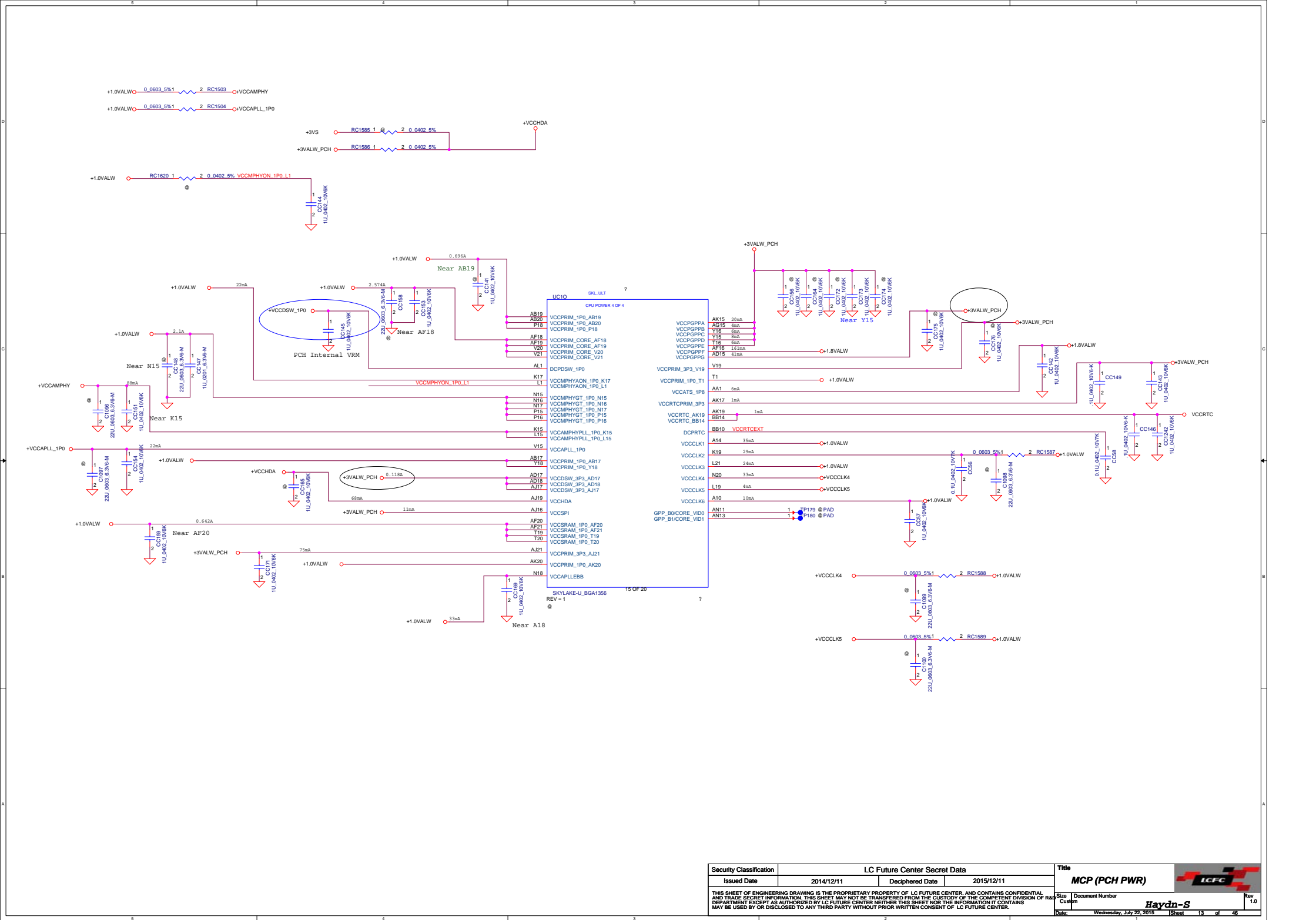
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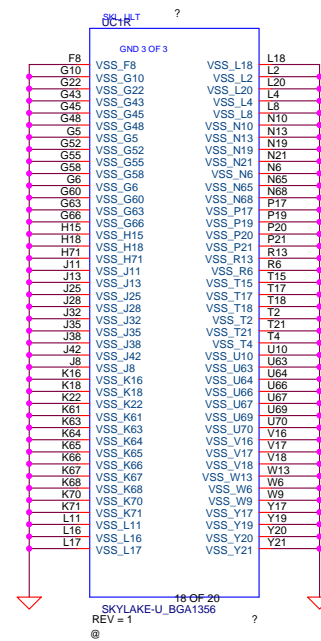
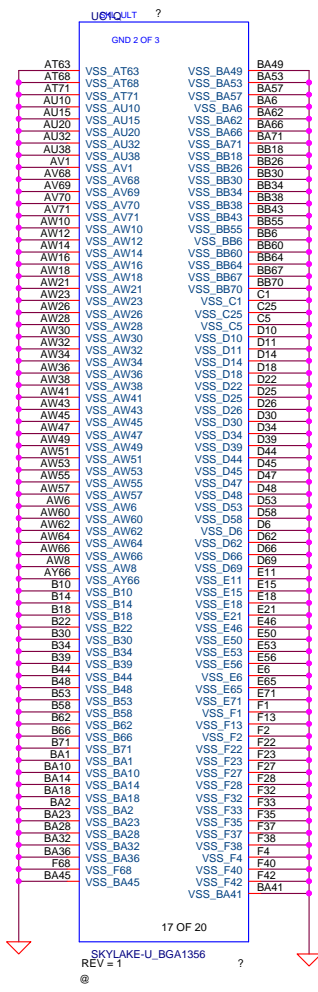
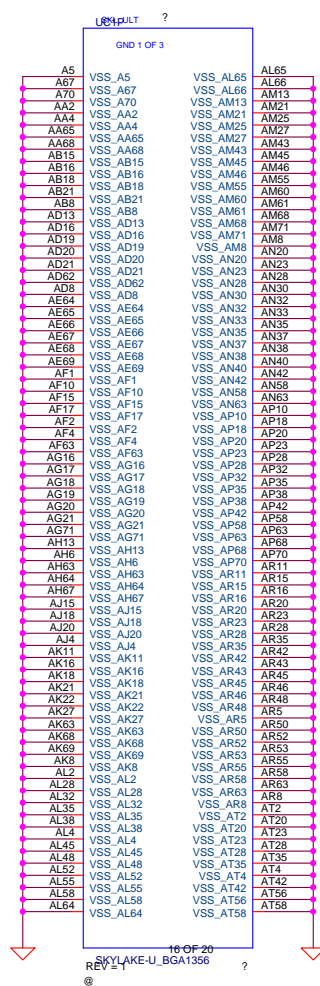



Title			
MCP (CSI2,EMMC,CLOCK)			
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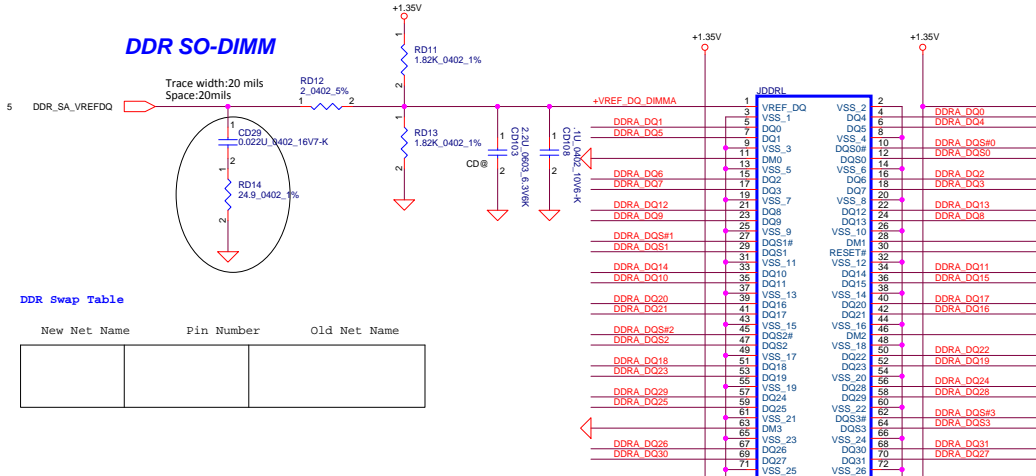




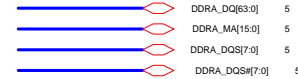


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DDR SO-DIMM



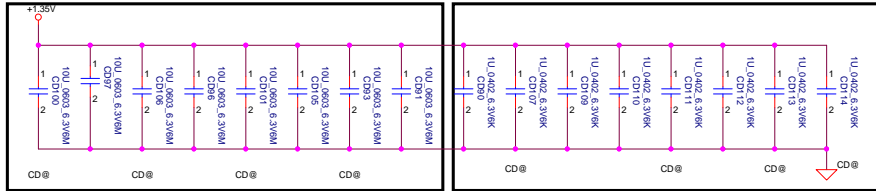
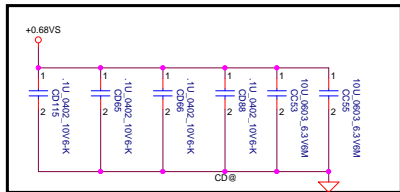
For RF request



DDR_SA_VREFDQ 5
DDR_SA_VREFDQ 5
DDR_SA_VREFDQ 5
DDR_SA_VREFDQ 5

VDDQ(2A)
Decoupling CAP
4 PCS 1UF CAP Near Each Side of DIMM VDD Pin
4PCS 10UF CAP Near Each Side of DIMM VDD Pin

VTT(700mA)
Decoupling CAP
4PCS 0.1UF CAP Near The DIMM
2PCS 10UF CAP On the VTT Island



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N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

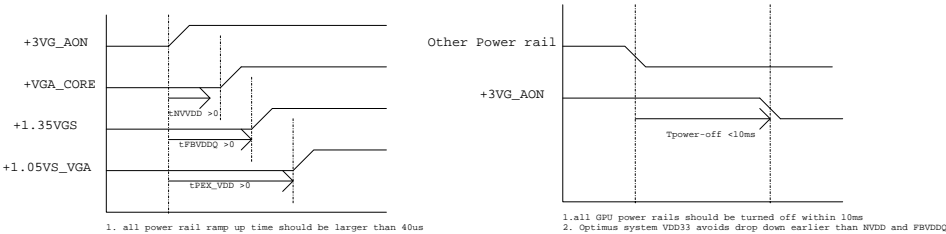
Products	GPU (4)	Mem (1.5)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)		(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

N15x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

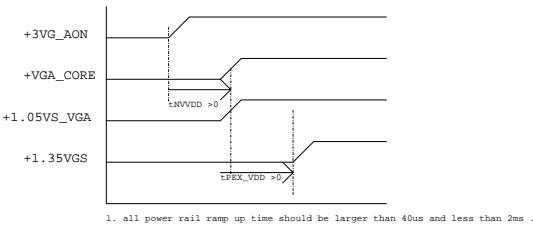
N15V-GM Power Sequence

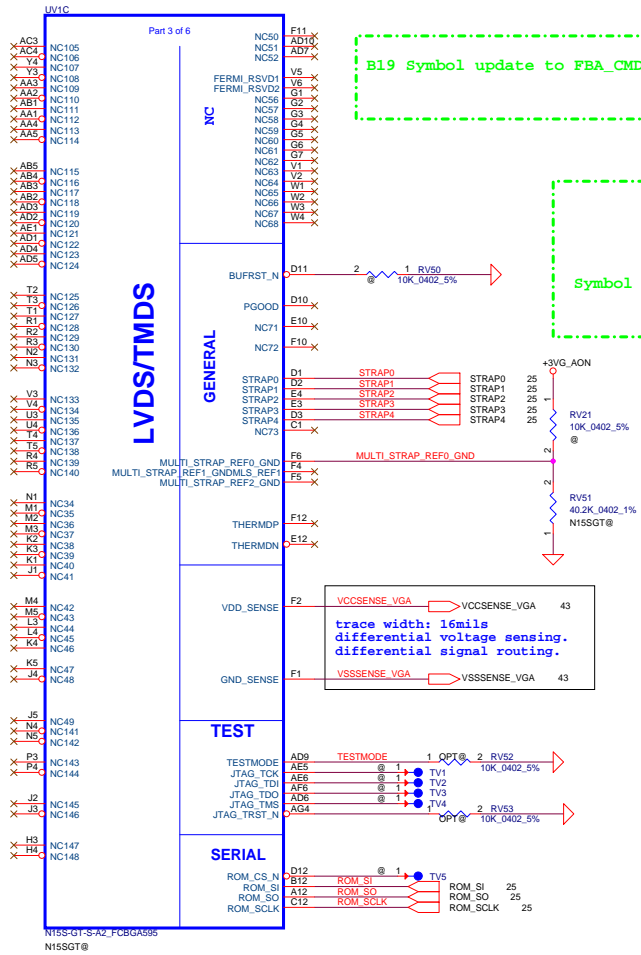


N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

N15S-GT Power Sequence

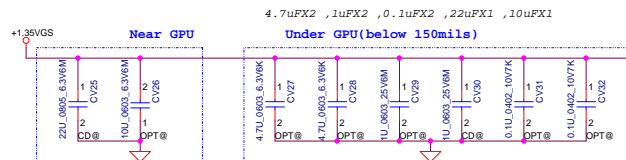




B19 Symbol update to FBA_CMD32

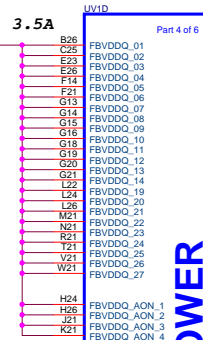
Symbol update to GPIO8

VCCSENSE_VGA VCCSENSE_VGA 43
trace width: 16mils
differential voltage sensing.
differential signal routing.



4.7uFX2, 1uFX2, 0.1uFX2, 22uFX1, 10uFX1

Symbol update to FBVDDQ_AON
H24/H26/J21/K21



POWER

2000mA

Near GPU

4.7uFX1, 1uFX1, 22uFX1, 10uFX1

Under GPU(below 150mils)

PEX_IQVDD/Q Decoupling

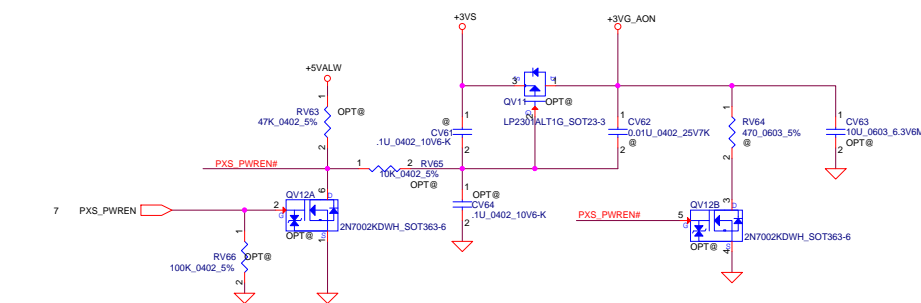
MLCC	N15S-GT
1.0uF	1
4.7uF	1
10uF	1
22uF	1

Symbol update to 3V3_AON

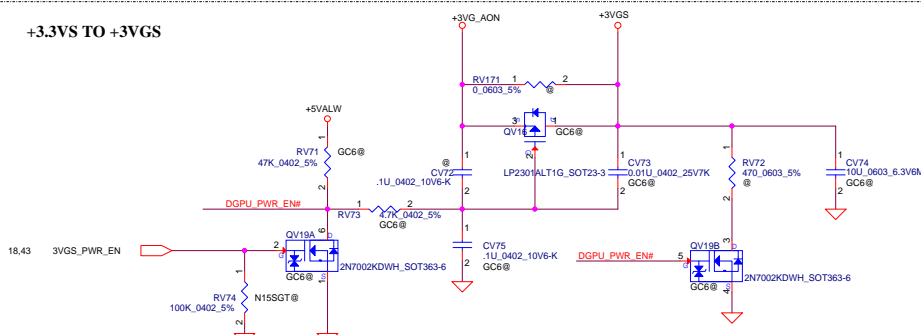
Place near balls(Under GPU) Place near GPU

CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2ohm
FB_CAL_x_PU_GND	42.2ohm
FB_CAL_xTERM_GND	51.1ohm

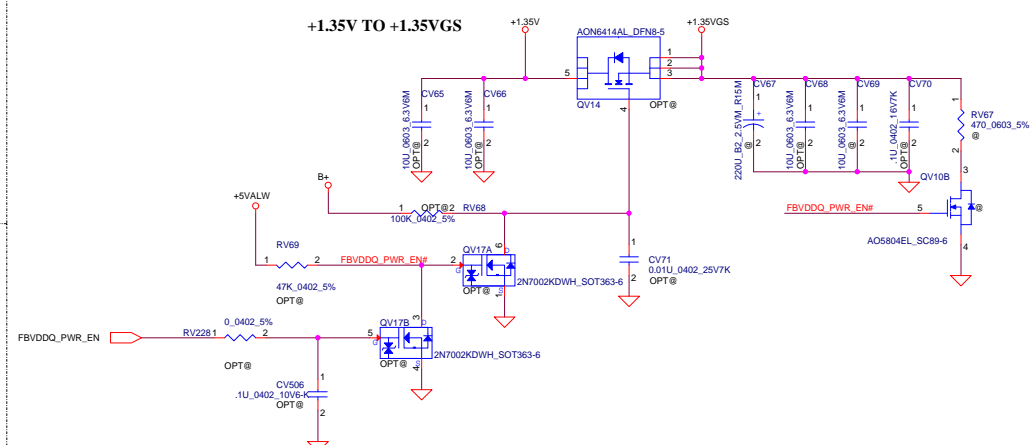
+3.3VS TO +3VG_AON

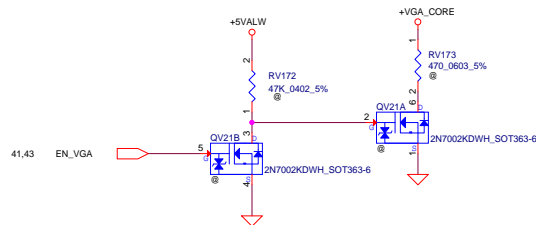
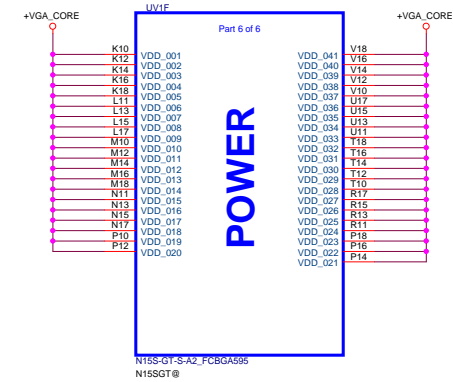
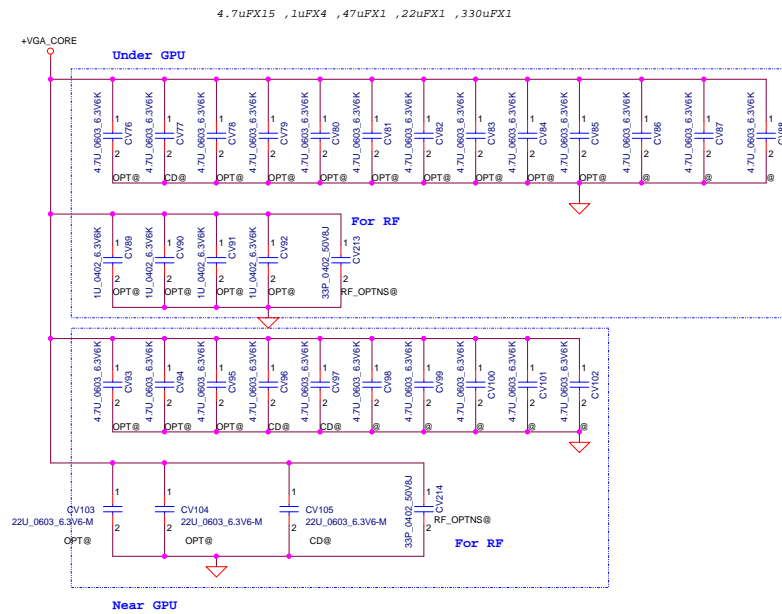
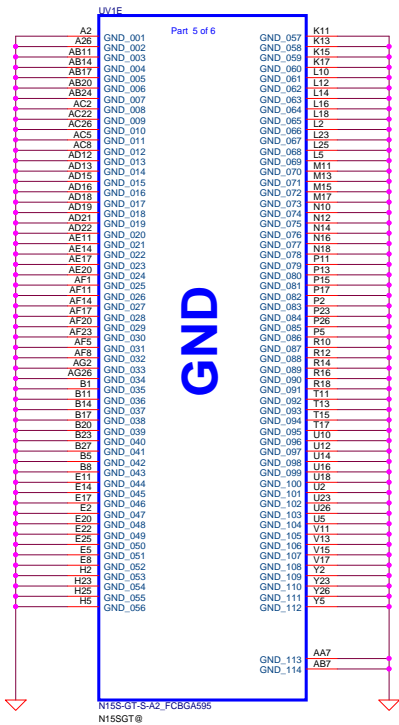


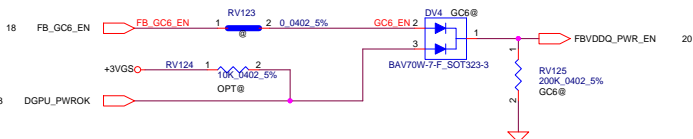
+3.3VS TO +3VGS



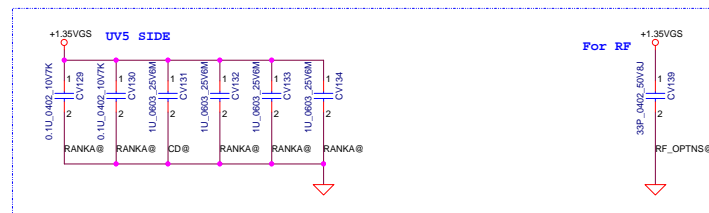
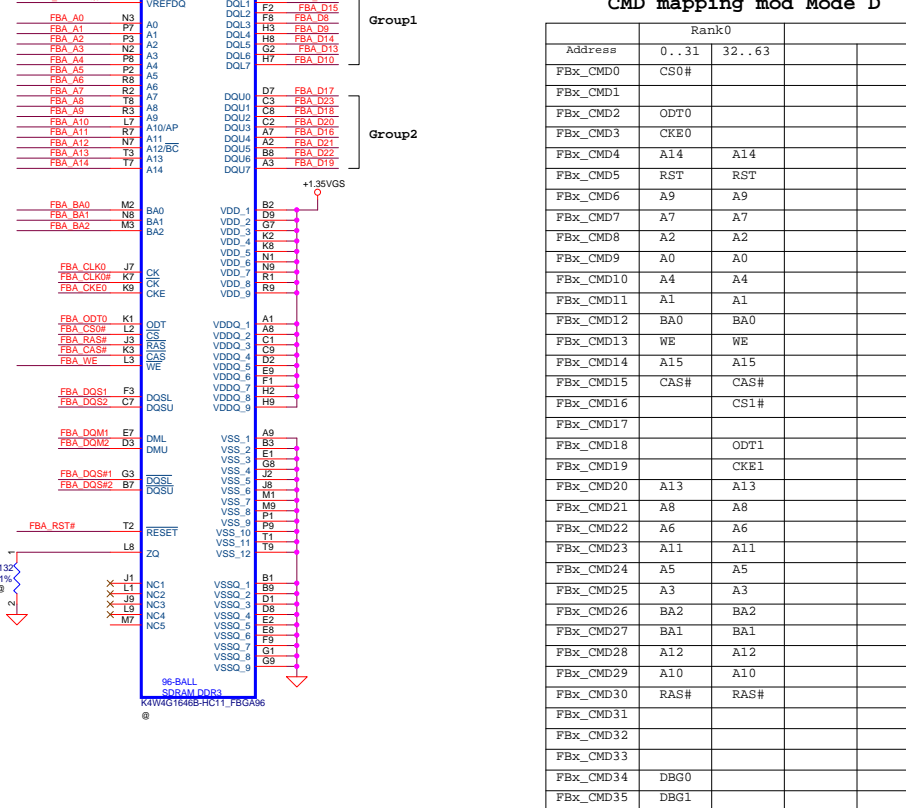
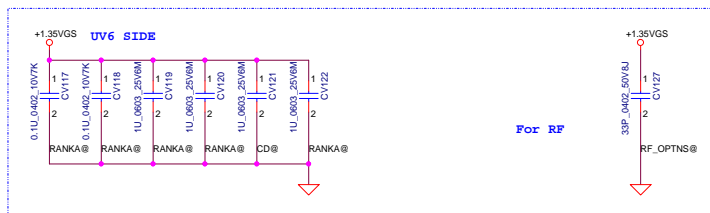
+1.35V TO +1.35VGS







1.0

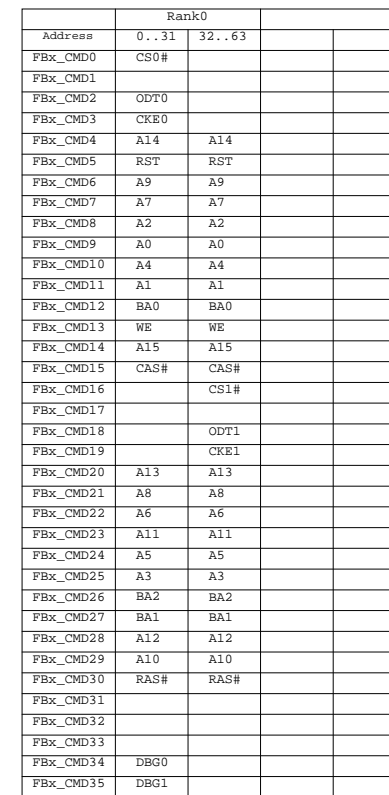
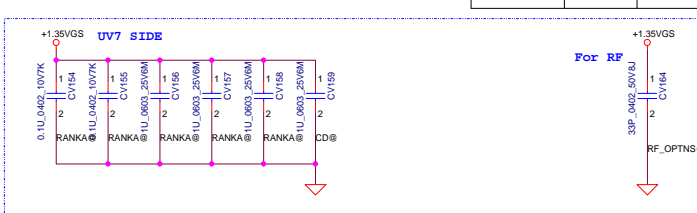
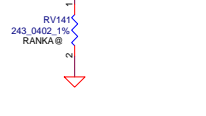


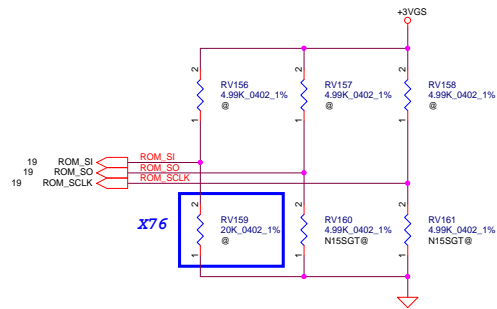
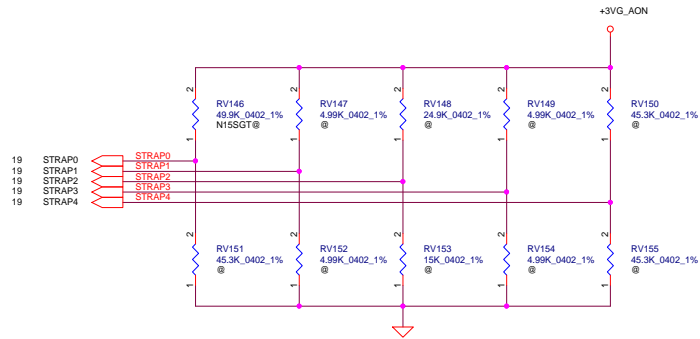
UV8 SIDE

0.1uF 0.402 107K Cv142
1uF 0.003 2506M Cv143
1uF 0.003 2506M Cv144
1uF 0.003 2506M Cv145
1uF 0.003 2506M Cv146
1uF 0.003 2506M Cv147

RANKA@
RANKA@
CD@
RANKA@
RANKA@
RANKA@

+1.35VGS





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

DEVID_SEL

0	(Default)
1	

PCIE_CFG

0	(Default)
1	

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

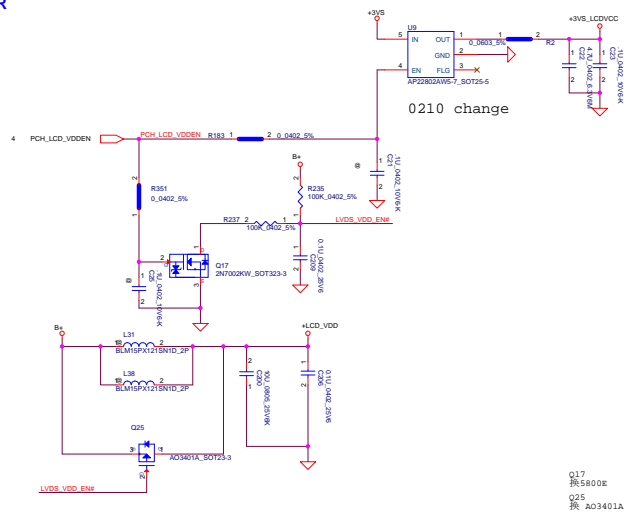
VGA_DEVICE

0	3D Device (Class Code 302h)
1	VGA Device (Default)

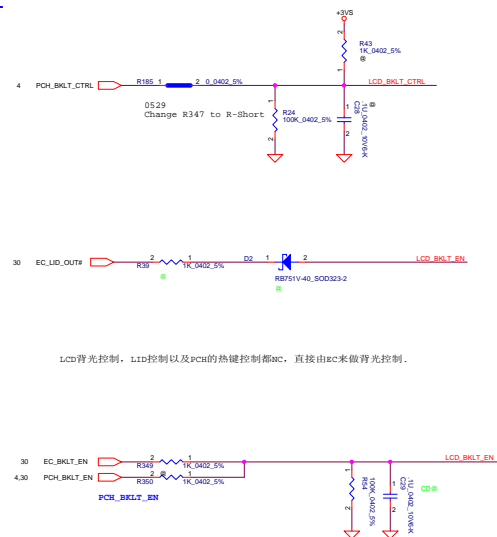
X76

GPU	FB Memory (DDR3)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GT	Hynix 900MHz	H5TC4G63CFR-N0C	0x2	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff
		256M x 16	PD 15K						
	Micron 900MHz	MT41J256M16HA-093G:E	0x4						
		256M x 16	PD 24.9K						
	Samsung 900MHz	K4W4G1646E-BC1A	0x1						
		256M x 16	PD 10K						
	Hynix 900MHz	H5TC2G63FFR-11C	0x9						
		128M x 16	PU 10K						
	Micron 900MHz	MT41J128M16JT-093G:K	0xA						
		128M x 16	PU 15K						
	Samsung 900MHz	K4W2G1646Q-BC1A	0xB						
		128M x 16	PU 20K						

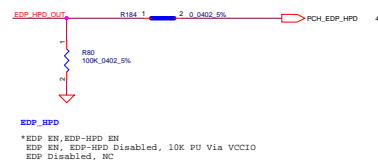
VRAM	X76	VRAM P/N
Samsung	X7607312002	SA000063F20
Micron	X7607312003	SA000060I10
Hynix	X7607312001	SA00007DU10



BKLT CNTL

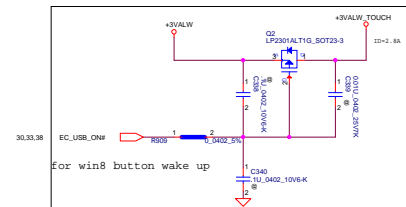
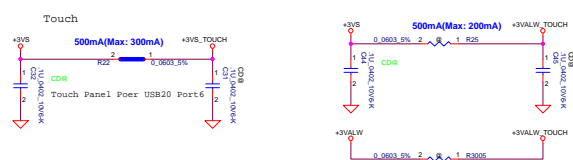
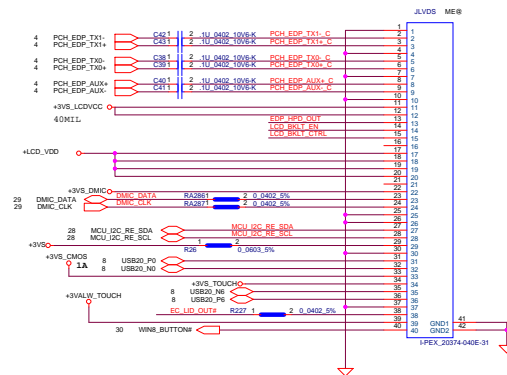


LCD背光控制, LID控制以及PCH的热键控制都NC, 直接由EC来做背光控制.

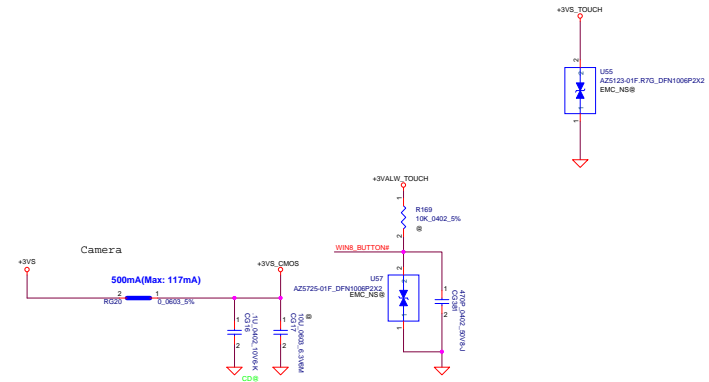
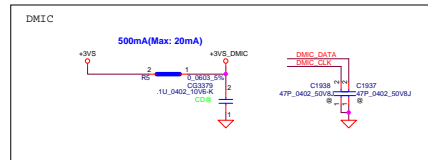
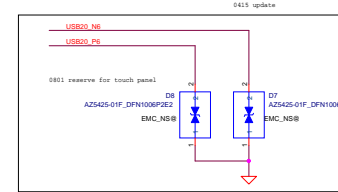



```
*EDP EN,EDP-HPD EN
EDP EN, EDP-HPD Disabled, 10K PU Via VCCIO
EDP Disabled, NC
```

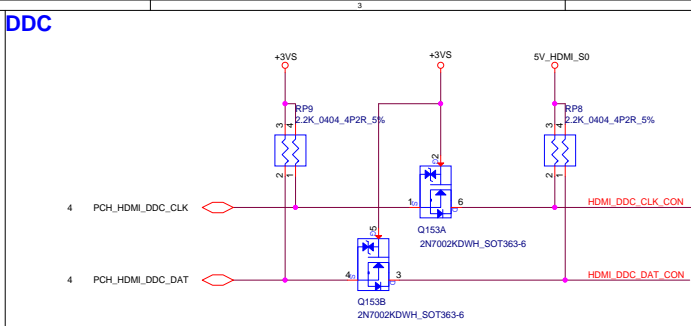
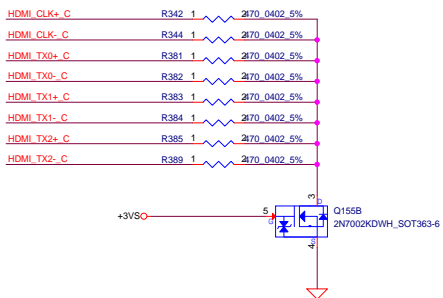
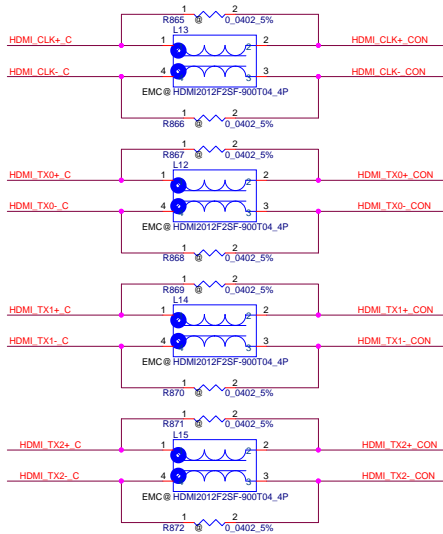
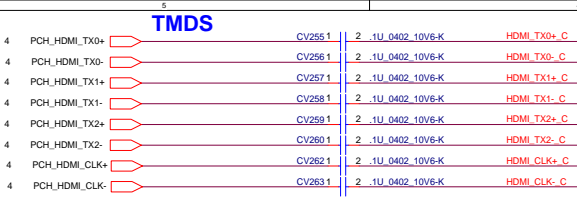
For LCD CONN YOGA3_11 "



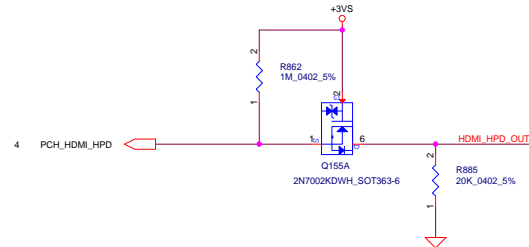
```
for win8 button wake u
```



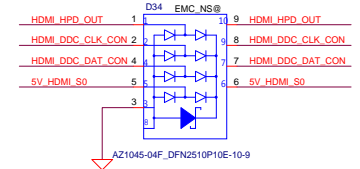
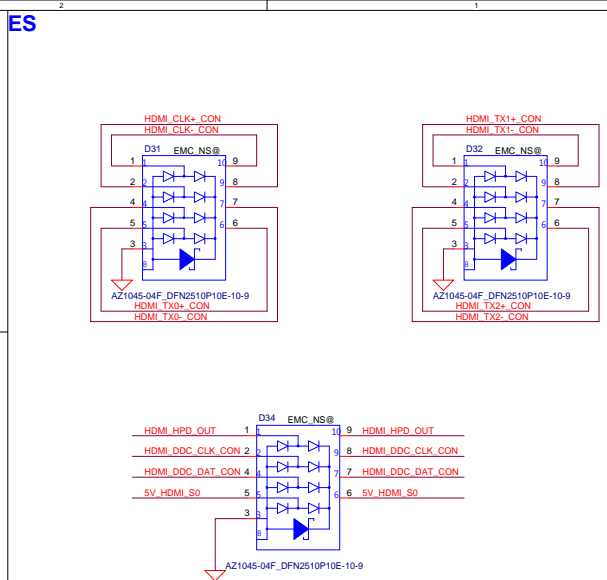
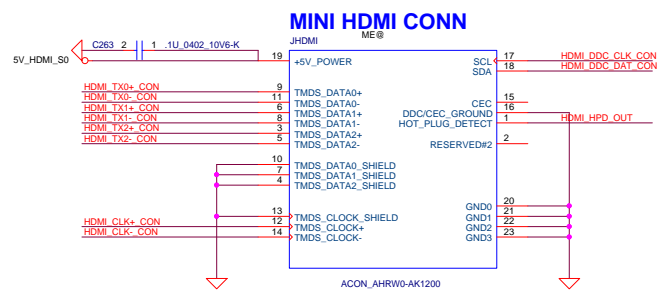
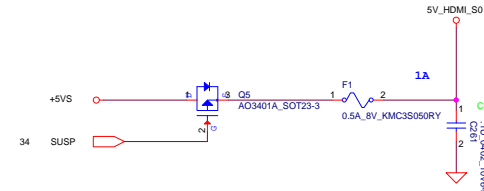
Security Classification	LC Future Center Secret Data			LCF	
Issued Date	2014/01/11	Deciphered Date	2013/11/08		
<p>THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THESE DRAWINGS ARE TO BE KEPT UNDER THE STRICTEST CONTROL BY THE DEPARTMENT OF DEFENSE EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>					
				Date: Wednesday, July 22, 2015	Page: 28 of 46

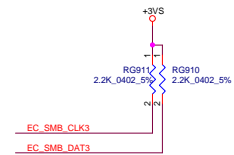
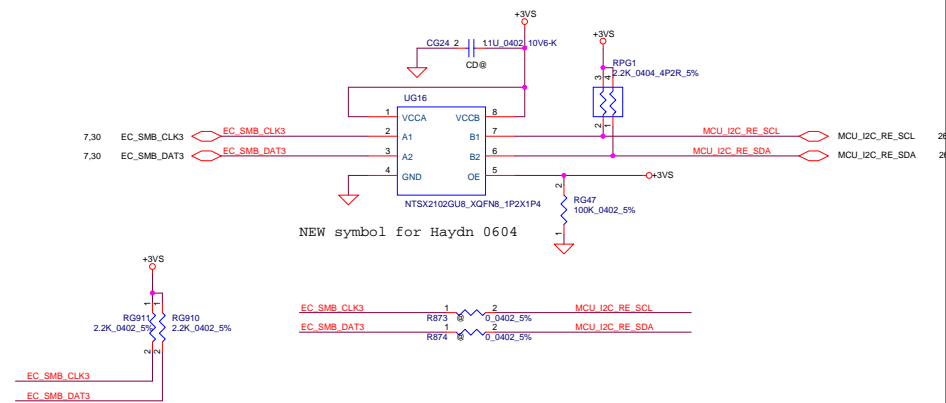


H-PLUG



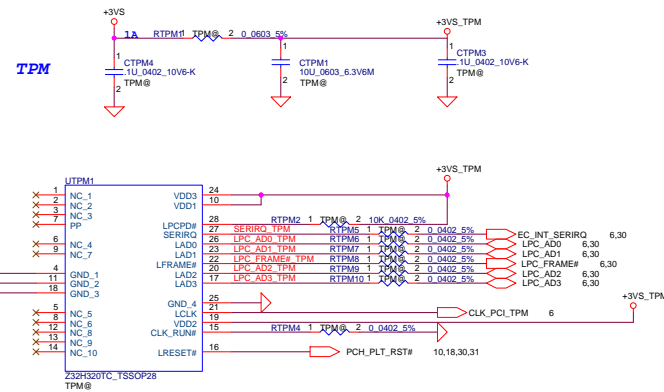
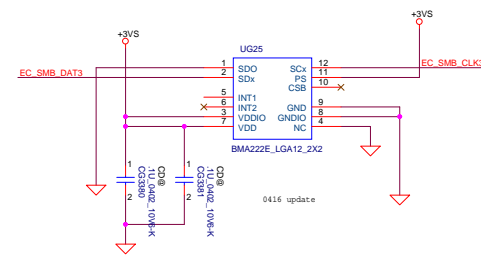
CONN



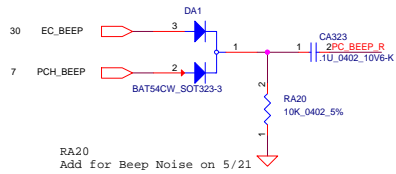


When use ISH change RG911/RG910 to 1K

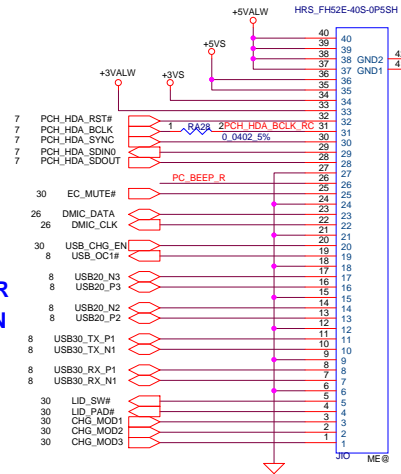
G-SENSOR



JIO HDA CARDREADER USB CONN

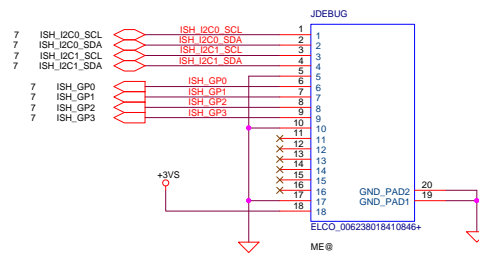
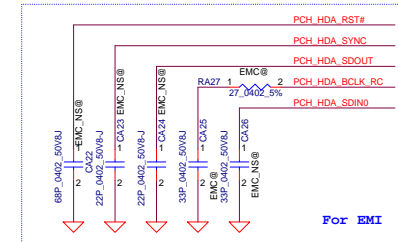
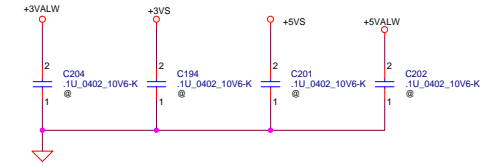


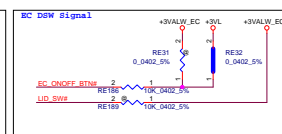
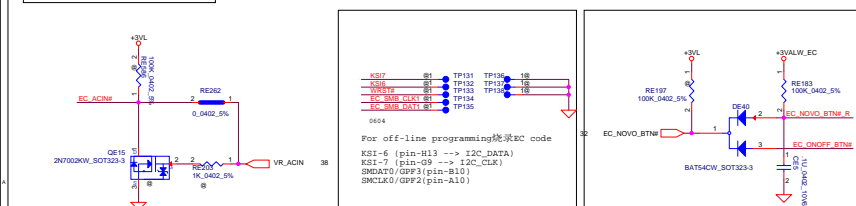
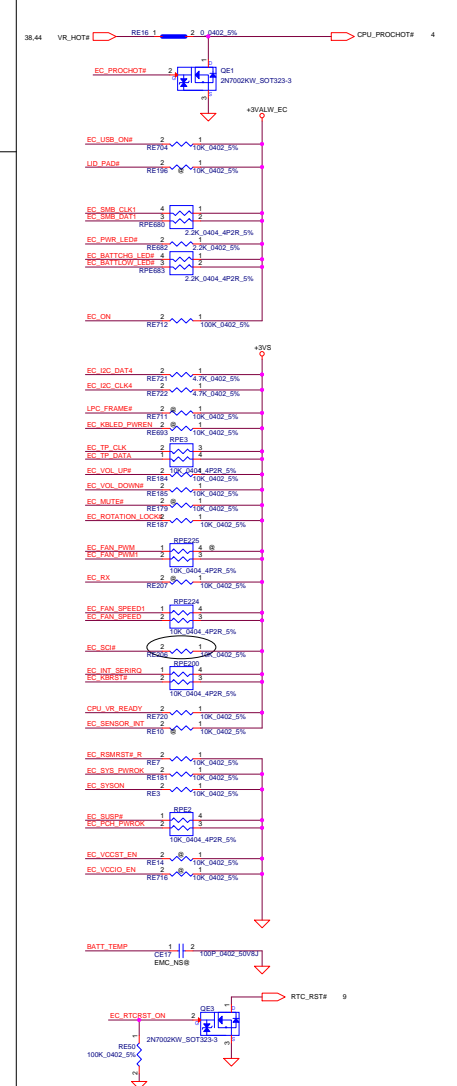
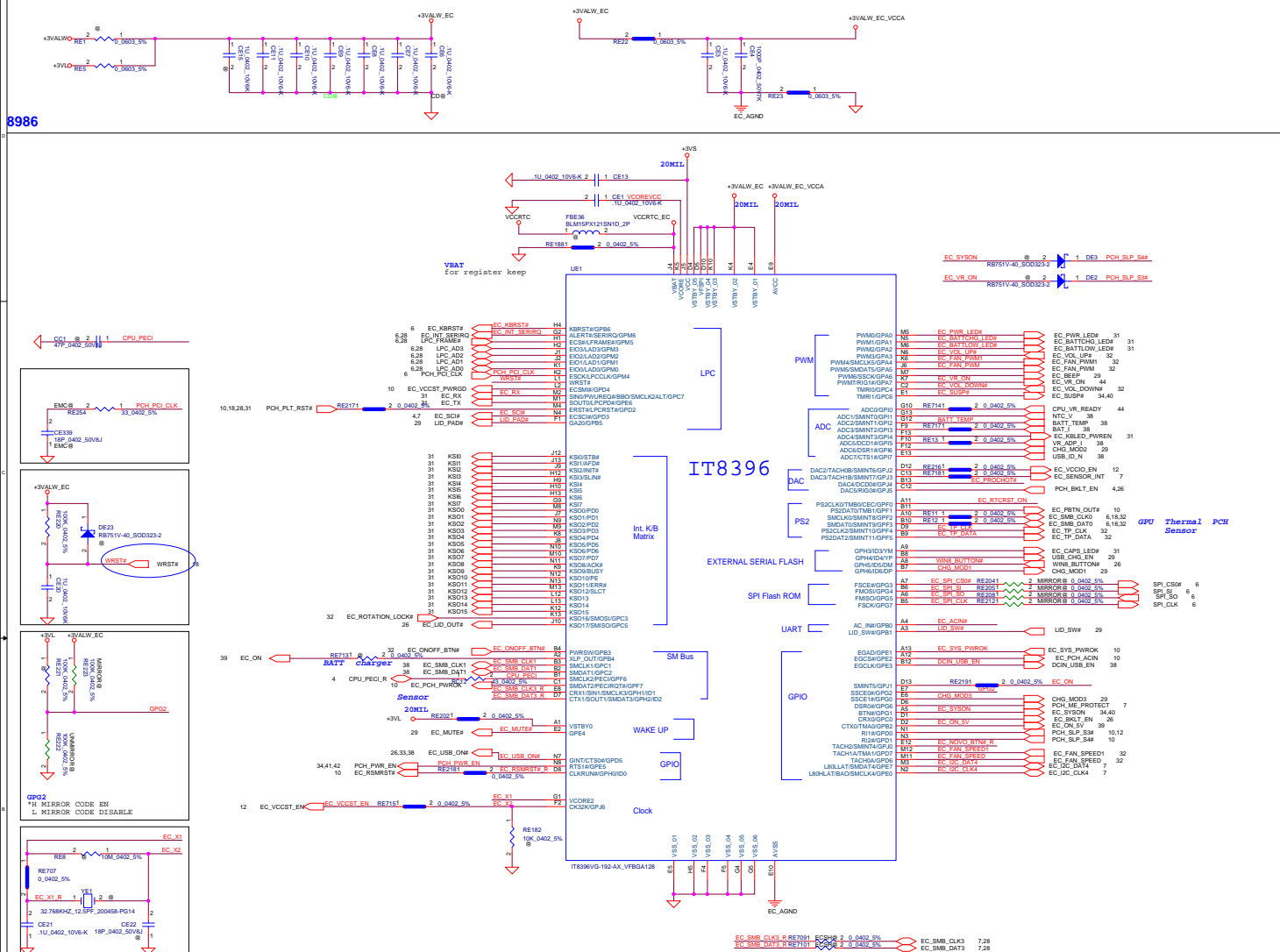
**CARD READER
Left USB_CONN**




RA28 Close to JIO

NEW symbol for Haydn 0609



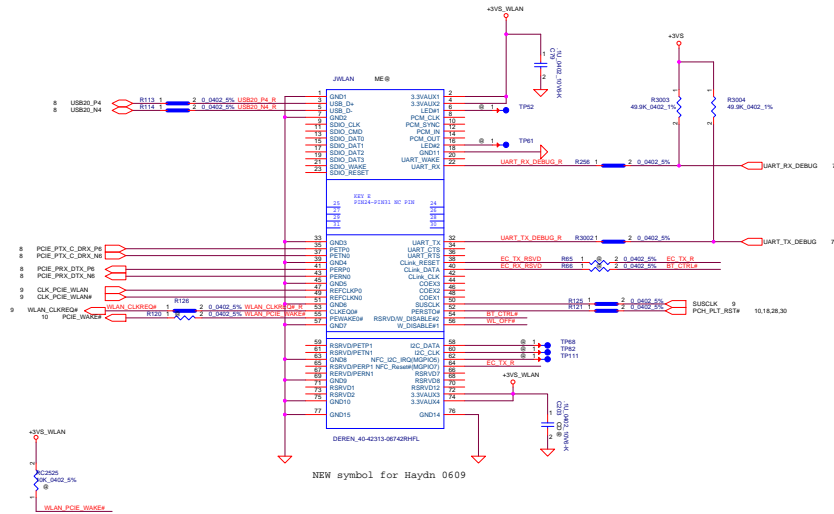
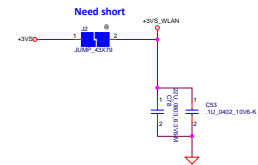


Security Classification	LC Future Center Secret Data		Title	ECIT8396		
Issued Date	2014/01/11	Deciphered Date	2013/11/08			

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WIFI&BT Board Connector
Mini Card(WLAN/WiMAX)

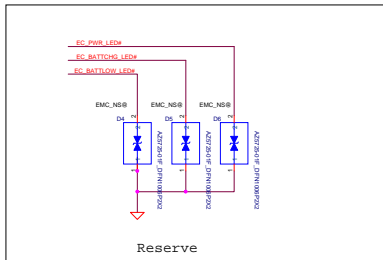
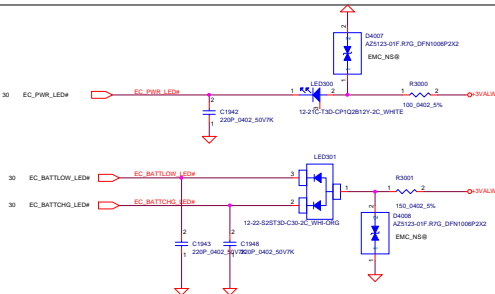
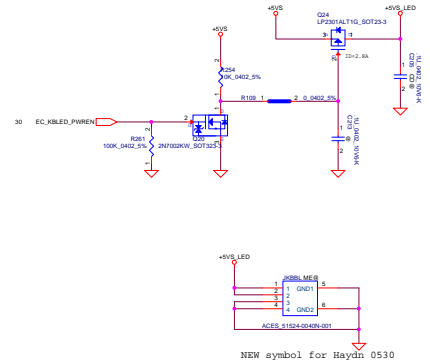


WLAN&BT Combo module circuits

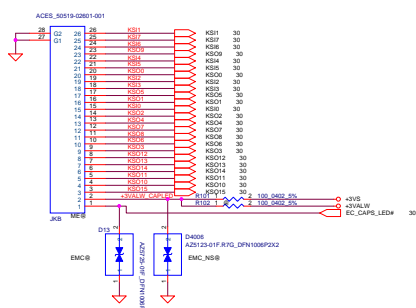
	BT on module Enable	BT on module Disable
BT_CTRL	H	L
PCH_BT_CN#	L	H



KB BL

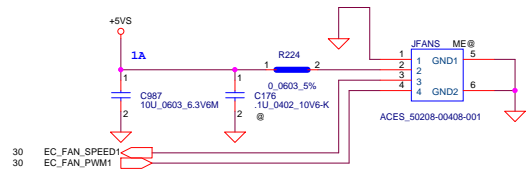
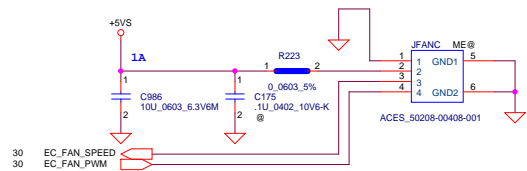


Keyboard Connector



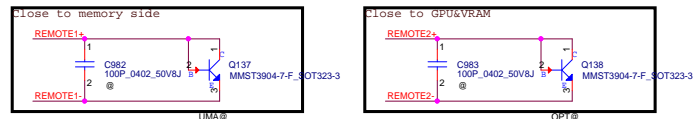
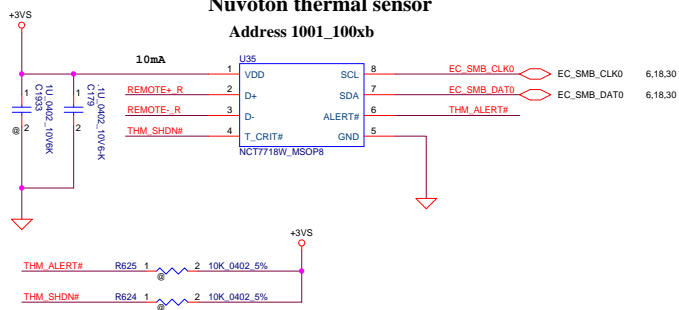
*WLAN CAPLED	C117	1	2	EMC_NSR	100P_0402_50VU	EC_CAPLED	C133	1	2	EMC_NSR	100P_0402_50VU
K500	C80	1	2	EMC_NSR	100P_0402_50VU	K501	C80	1	2	EMC_NSR	100P_0402_50VU
K504	C82	1	2	EMC_NSR	100P_0402_50VU	K507	C83	1	2	EMC_NSR	100P_0402_50VU
K506	C84	1	2	EMC_NSR	100P_0402_50VU	K509	C85	1	2	EMC_NSR	100P_0402_50VU
K508	C86	1	2	EMC_NSR	100P_0402_50VU	K512	C87	1	2	EMC_NSR	100P_0402_50VU
K513	C88	1	2	EMC_NSR	100P_0402_50VU	K515	C89	1	2	EMC_NSR	100P_0402_50VU
K519	C100	1	2	EMC_NSR	100P_0402_50VU	K524	C109	1	2	EMC_NSR	100P_0402_50VU
K511	C110	1	2	EMC_NSR	100P_0402_50VU	K517	C112	1	2	EMC_NSR	100P_0402_50VU
K510	C107	1	2	EMC_NSR	100P_0402_50VU	K518	C112	1	2	EMC_NSR	100P_0402_50VU
K503	C116	1	2	EMC_NSR	100P_0402_50VU	K519	C108	1	2	EMC_NSR	100P_0402_50VU
K504	C115	1	2	EMC_NSR	100P_0402_50VU	K514	C123	1	2	EMC_NSR	100P_0402_50VU
K50	C121	1	2	EMC_NSR	100P_0402_50VU	K509	C111	1	2	EMC_NSR	100P_0402_50VU
K500	C124	1	2	EMC_NSR	100P_0402_50VU	K511	C120	1	2	EMC_NSR	100P_0402_50VU

For EMC

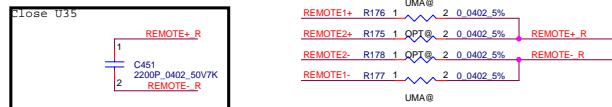


Nuvoton thermal sensor

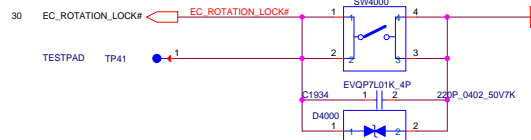
Address 1001_100xb



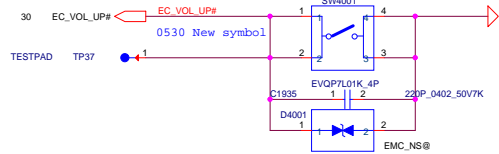
REMOVED1+/-:
Trace width/space:10/10 mil
Trace length:<8"



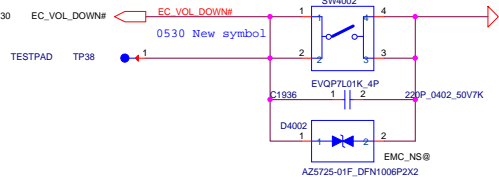
Rotation button



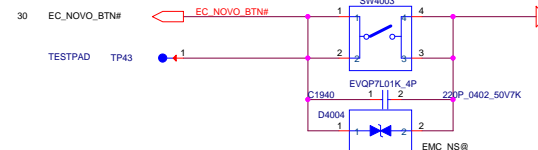
Vol up/down button



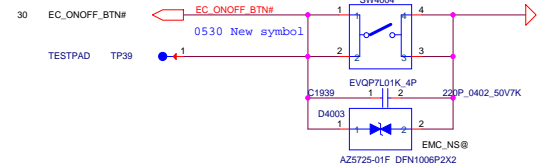
Vol up/down button



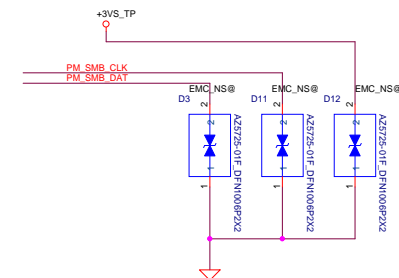
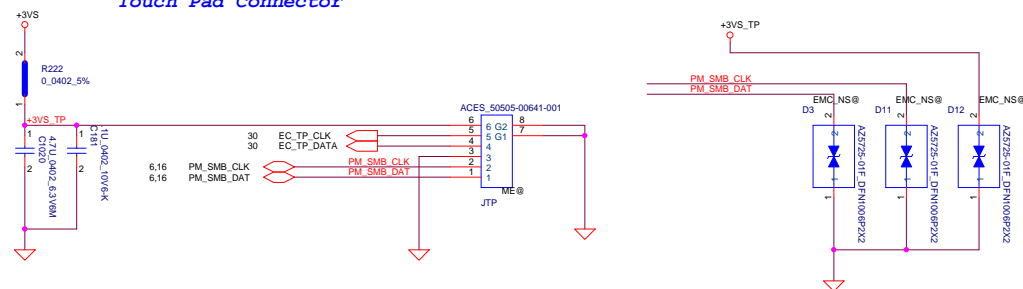
NOVO button

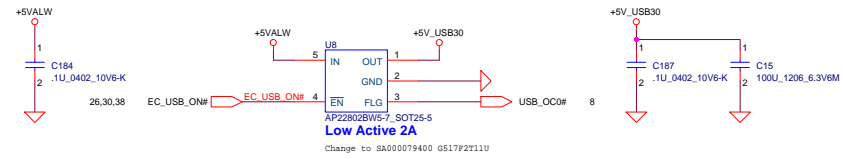
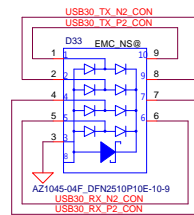
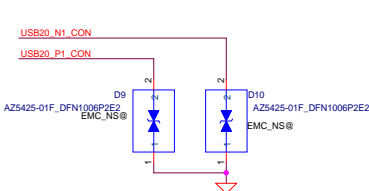
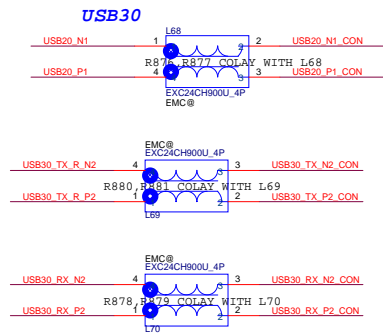


ON/OFF button

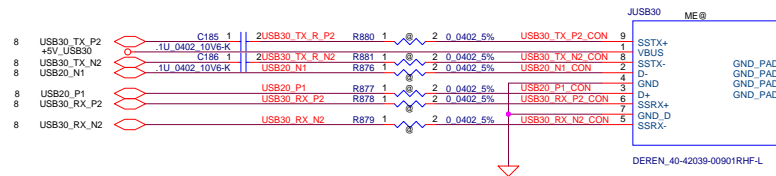


Touch Pad Connector

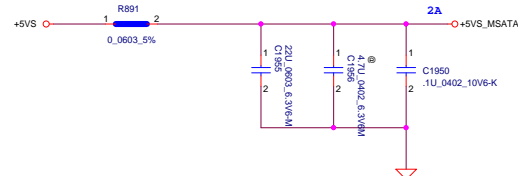
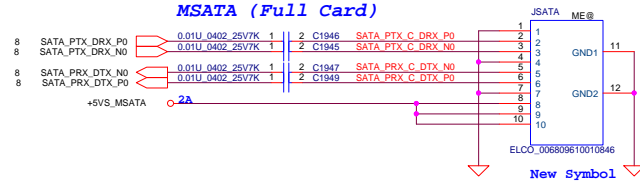
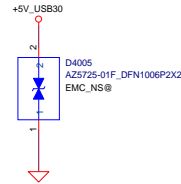


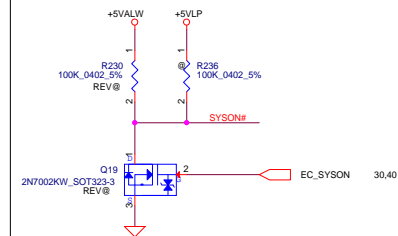


Left USB3.0/2.0

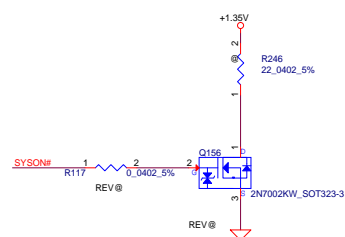
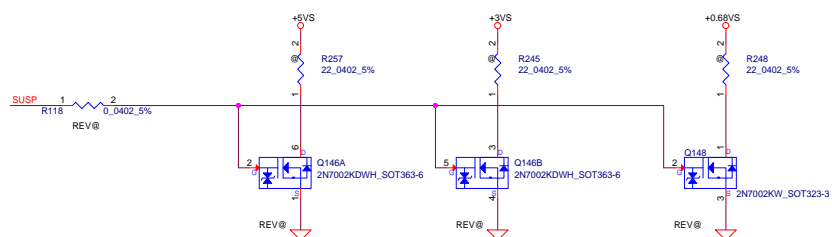
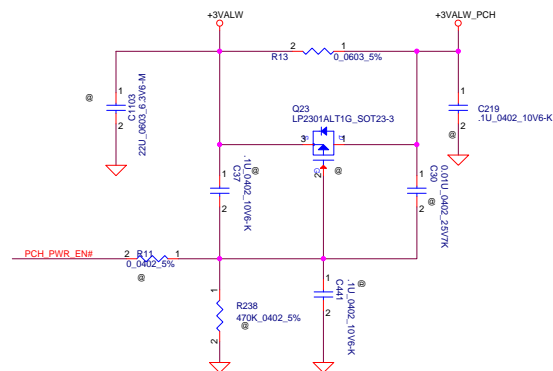
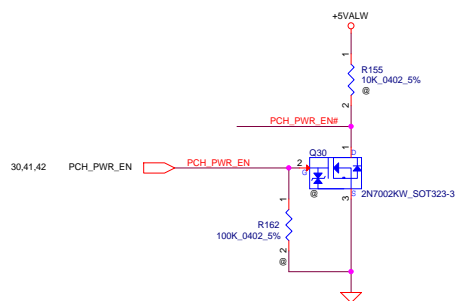


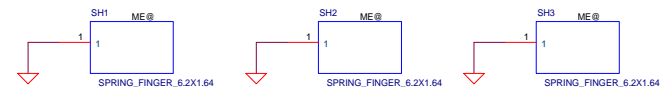
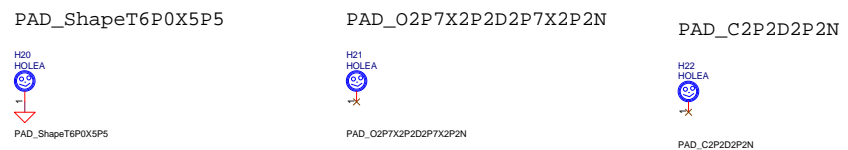
NEW symbol for Haydn 0604






For High speed signal cross moat concern.





Security Classification		LC Future Center Secret Data		Title			
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SDV

1/19:
1.Firstly initial

1/21:
1.PCH ISH reserve sensor solution

1/22:
1.U8 USB power switch change to AP22802BW5-7_SOT25-5
from AP2820CMMTR-G1_MSOP8

1/28:
1.EC change to IT8986 from IT8386

2/4
1.EC_ON change to GPJ1
2.GPU 1.05VGS source change to +1.0VALW
3.BAT_I change to GPI3
4.CPU_VR_READY change to GPI0
5.EC_VR_ON change to GPA7
6.EC_VCCIO_EN change to GPJ2
7.VGA_AC_DET change to GPJ3
8.VGA 1.05VGS HW load switch del

2/9
1.Add VDDQ_PGOOD to EC GPJ3

2/10
1.RC138,QC6,RC136 change to unmount
2.RC1599 change to mount
3.U9 change to AP22802AW5-7_SOT25-5 from AP2821KTR-G1_SOT23-5

2/11 **
1.Add SH1/SH2/SH3 shielding
2.RC1585 unmount,RC1586 mount

2/12
1.Del C224/C225/C217/C218/C226/C220
2.RC157/RC170 change to unmount
3.Del PR138,Add PR1015/PR1016
4.Del PD109/PD110 Add PD111
5.Add PR1017

2/13
1.Del TP203/TP172/TP173/TP177/TP178
2.Del UC8/RC1591/DC2/CC1247/JC2/CC1248
3.Del UC7/RC1590/DC3/CC1245/RC1592/CC1246
4.QC12/QC16 change to AO5804EL_SC89-6 from 2N7002KDWH_SOT363-6
5.QC13/QC14 change to DMG1012T-7_SOT523-3 from 2N7002KW_SOT323-3

2/24
1.JDDR1.181 change to DDRA_DQ56 from DDRA_DQ61
2.JDDR1.180 change to DDRA_DQ61 from DDRA_DQ56
3.JDDR1.191 change to DDRA_DQ62 from DDRA_DQ59
4.JDDR1.192 change to DDRA_DQ58 from DDRA_DQ62
5.JDDR1.194 change to DDRA_DQ59 from DDRA_DQ58
6.RC59 change to @

2/25
1.Add JDEBUB connector for Intel ISH debug
2.VRAM Hynix change to H5TC4G63CFR-N0C
3.VRAM Samsung change to K4W4G1646S-BC1A
4.CC165 change to @
5.CC57 change to luf from 0.luf and mount
6.U56 VIN1/VIN2,VOUT1/VOUT2 swap

2/28
1.Del TP197,TP198,TP200,TP40,TP141,TP44,TP189,TP191,TP196,
TP183,TP185,TP184,TP181,TP194,TP187,TP182,TP188,TP193,TP190,TP192,TP201,TP195,TP186,TP236

3/2 *****
1.Del RC1596,RC1597,Add RPC68
2.Change RPC4 to 10K_0404_4P2R_5% from 10K_0804_8P4R_5%
3.Change UV2 to 74LVC1G08SE-7_SOT353-5 from 74LVC1G08GW_SOT353-1-5

3/3
1.JDEBUB change to ELCO_006238018410846+
2.Reserve RE720 for CPU_VR_READY pull high +3VS
3.UTPM1 change to Z1Z320TC_TSSOP28 from ST332P24AR28PVSP_TSSOP28
4.RTPM2 change to 10K from 4.7K
5.Del RE214/RE215/RE708,Del RE690/RE691@
6.Add RE721/RE722 10K pull high +3VS
7.Del VDDQ_PGOOD Add EC_SENSOR_INT
8.WIN8_BUTTON# change to EC PIN A8, CHG_MOD1 change to EC PIN B7
9.Add EC_I2C_DAT4 to EC PIN M3, Add EC_I2C_CLK4 to EC PIN N2
10.Add RPC69/RC2533/RC2534/QC45

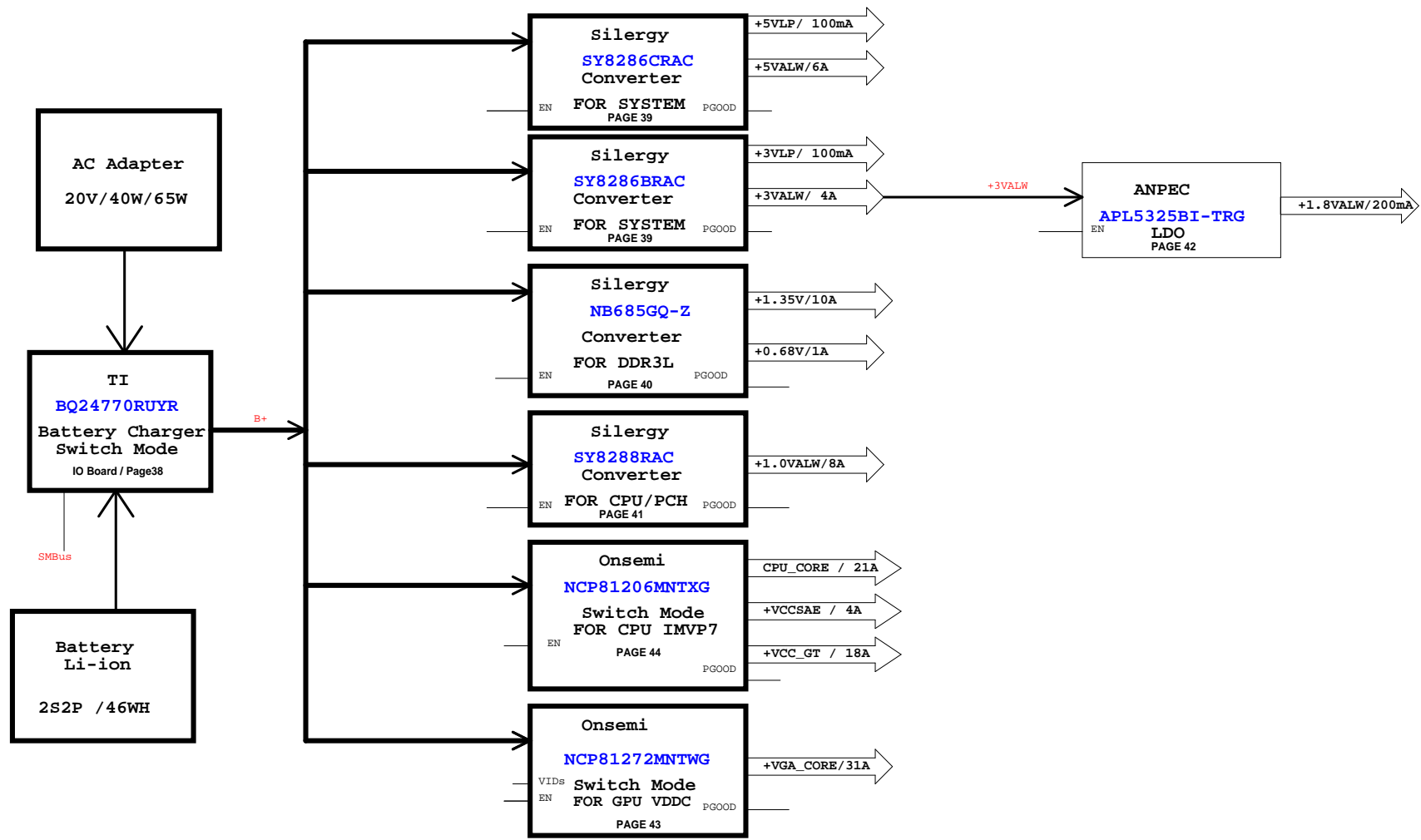
3/4
1.RE10 pin2 change to EC_SENSOR_INT from EC_ON_5V
2.Update JDEBUB symbol
3.Reserve CC1255, C1957/C1958/C226/C1959/C1960/C1961/C1962/C1963/C1964/C1965 for EMC

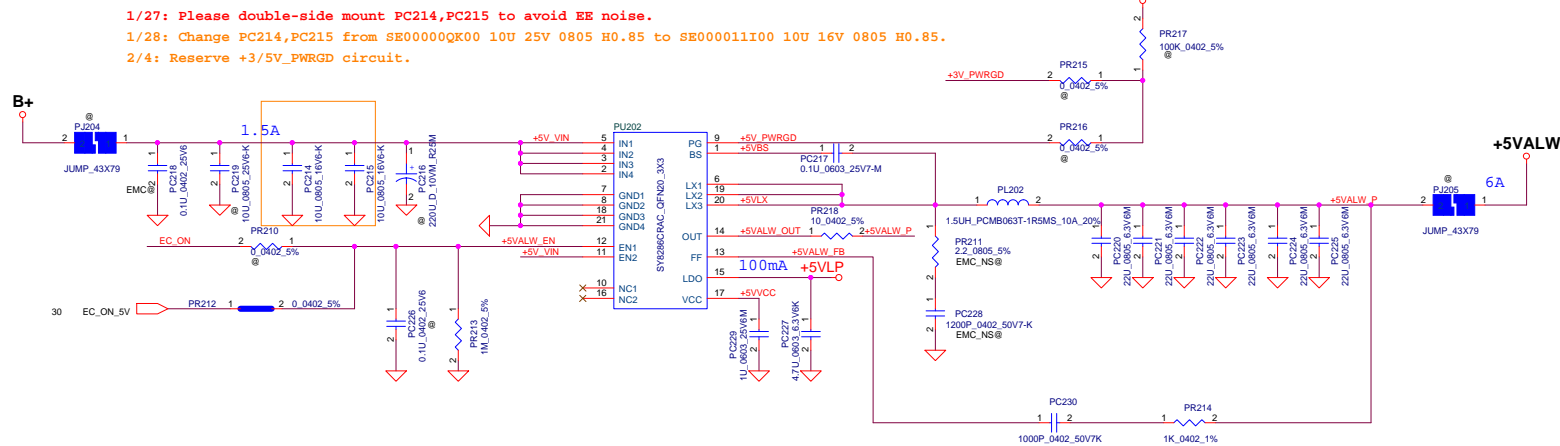
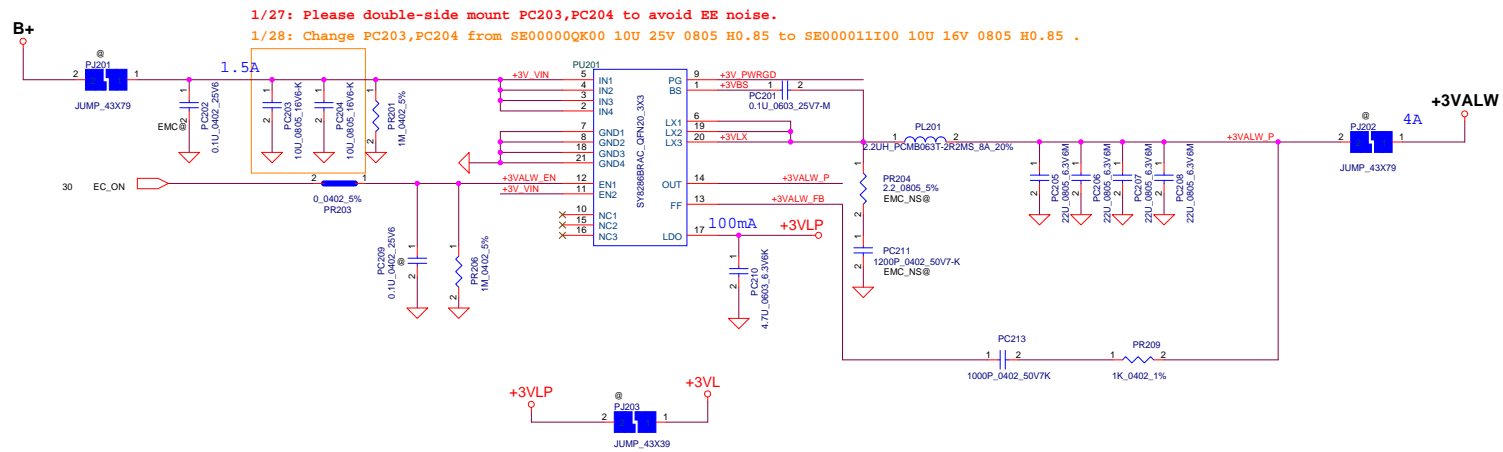
3/5
1.Del TP90/TP92

3/9
1.Add RC2535 0ohm, Add RC2536 1K to GND

3/10
1.H17 change to PAD_CT7P0ShapeB7P0X8P25D2P3 from PAD_C7P0D2P3

3/11
1.RC64 change to @ from ES@
2.CC23 change to @



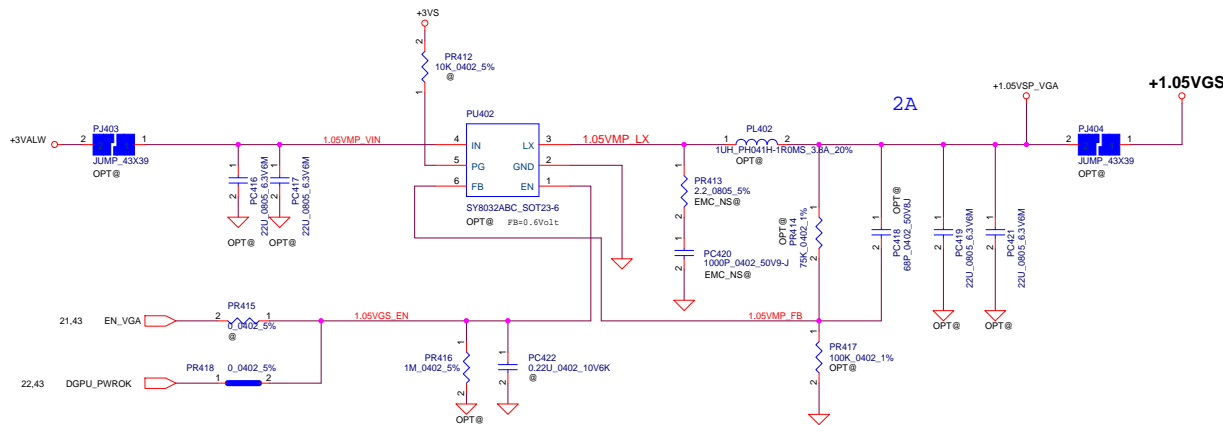
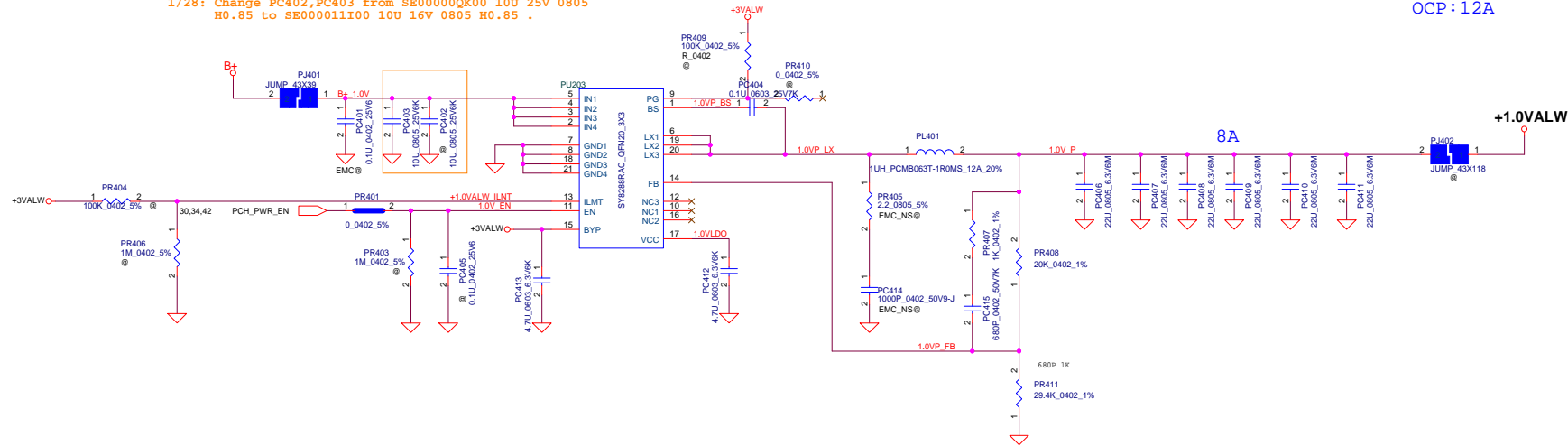


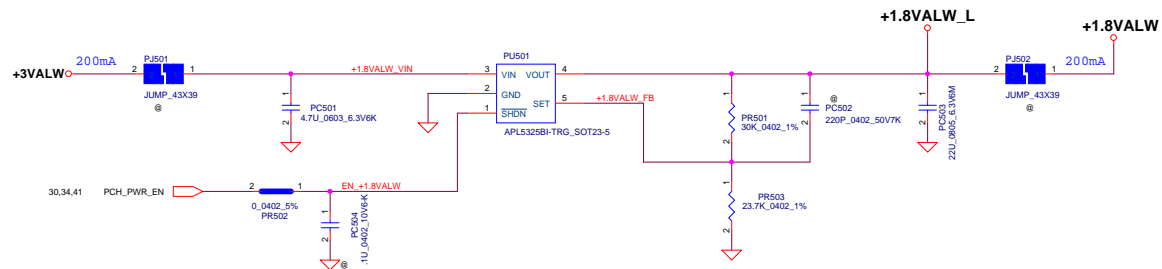
3VALWP VFB=2V TDC 5A Fsw=350KHZ OCP: 7.8A~9.5A	5VALWP TDC 5A Fsw=300KHZ OCP: 7.8A~9.5A
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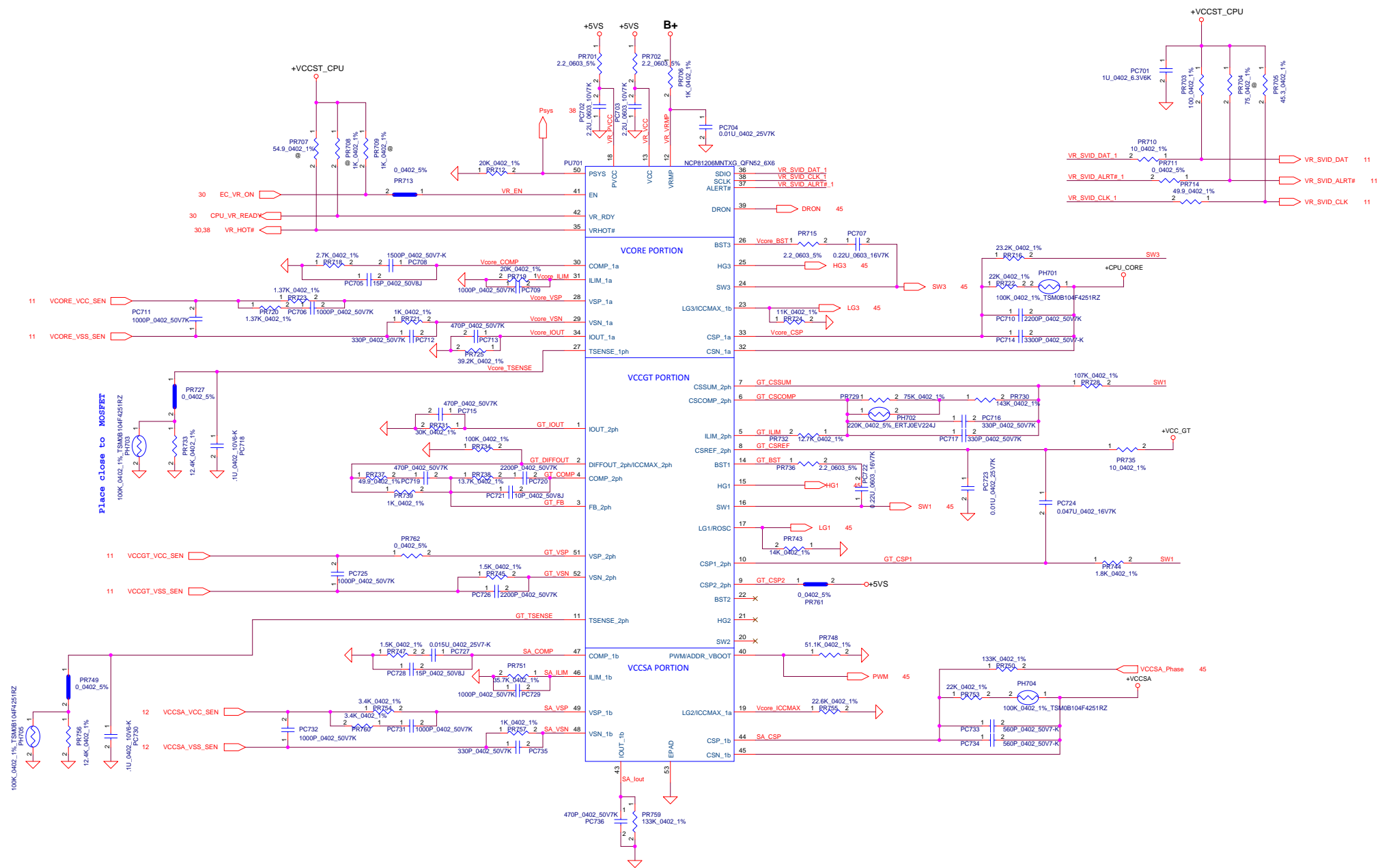
1/27: Please double-side mount PC402,PC403 to avoid EE noise.
1/28: Change PC402,PC403 from SE000000K00 10U 25V 0805 H0.85 to SE000011I00 10U 16V 0805 H0.85 .

Fsw=800KHZ
Vfb=0.6V
Vout=1.051V
OCP:12A





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